Frequency Synthesis & Signal Integrity

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ECE_5IC05_TP **ICS905 - FARE**

M2 « Integration Circuits & Systems »

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Summary

- **Digital Transceiver RF Front-end**
- Signal Integrity
- Frequency Synthesizers
- RF oscillators
- PLLs
- Indirect frequency synthesis

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Systems for wireless communications

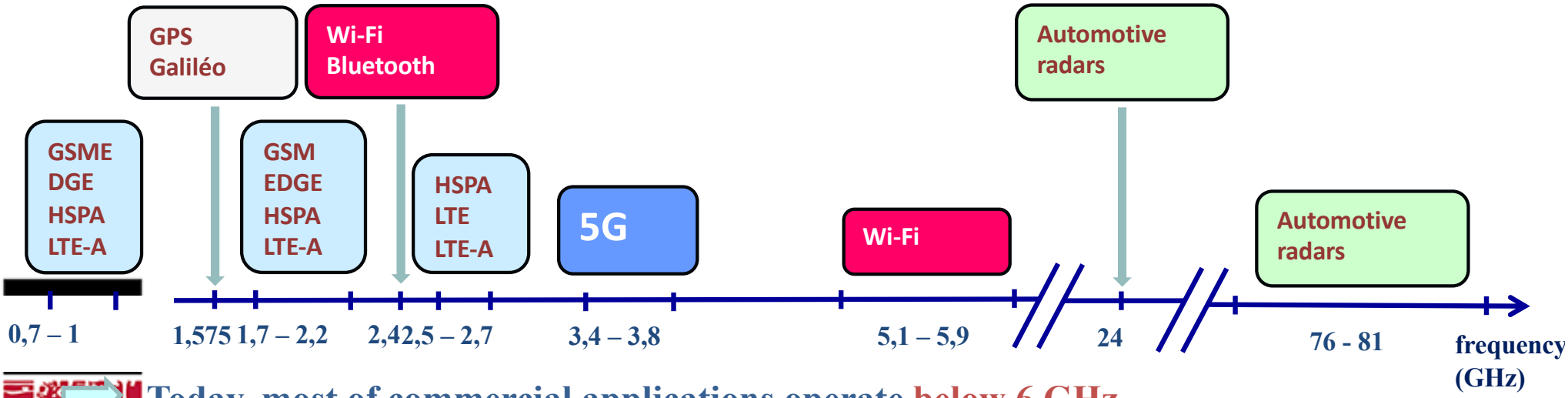
- 1 – Very high frequency of operation, typically 0,1 - 100 GHz = RF (Radio-Frequency)

  For commercial applications …

  – Wireless communications standards : GSM (2G), GPRS (2.5G), EDGE (2.75G), WCDMA (3G), HSPA (3.5G), LTE (3.9G or 4G), LTE-Advanced (4G or 4.5G), LTE-Advanced Pro (4.5 or 4.9G), 5G, Wi-Fi, Bluetooth, …

  – Geolocation systems (GPS, Galiléo)

  – Automotive radars



Today, most of commercial applications operate below 6 GHz

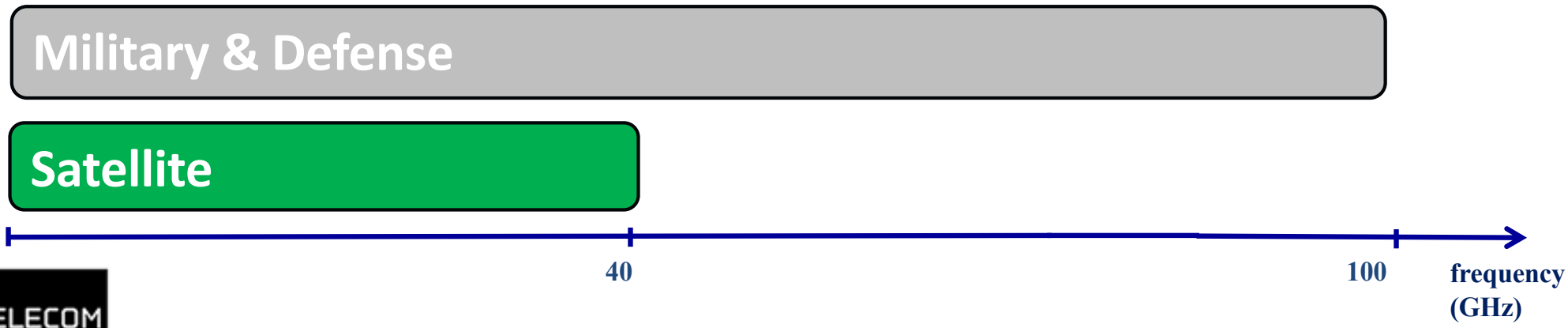
Systems for wireless communications

- 2 – Very high frequency of operation, typically 0,1 - 100 GHz = RF (Radio-Frequency)

For specific applications …

– Satellite communications : from 1 to 40 GHz approximately (discontinued spectrum)

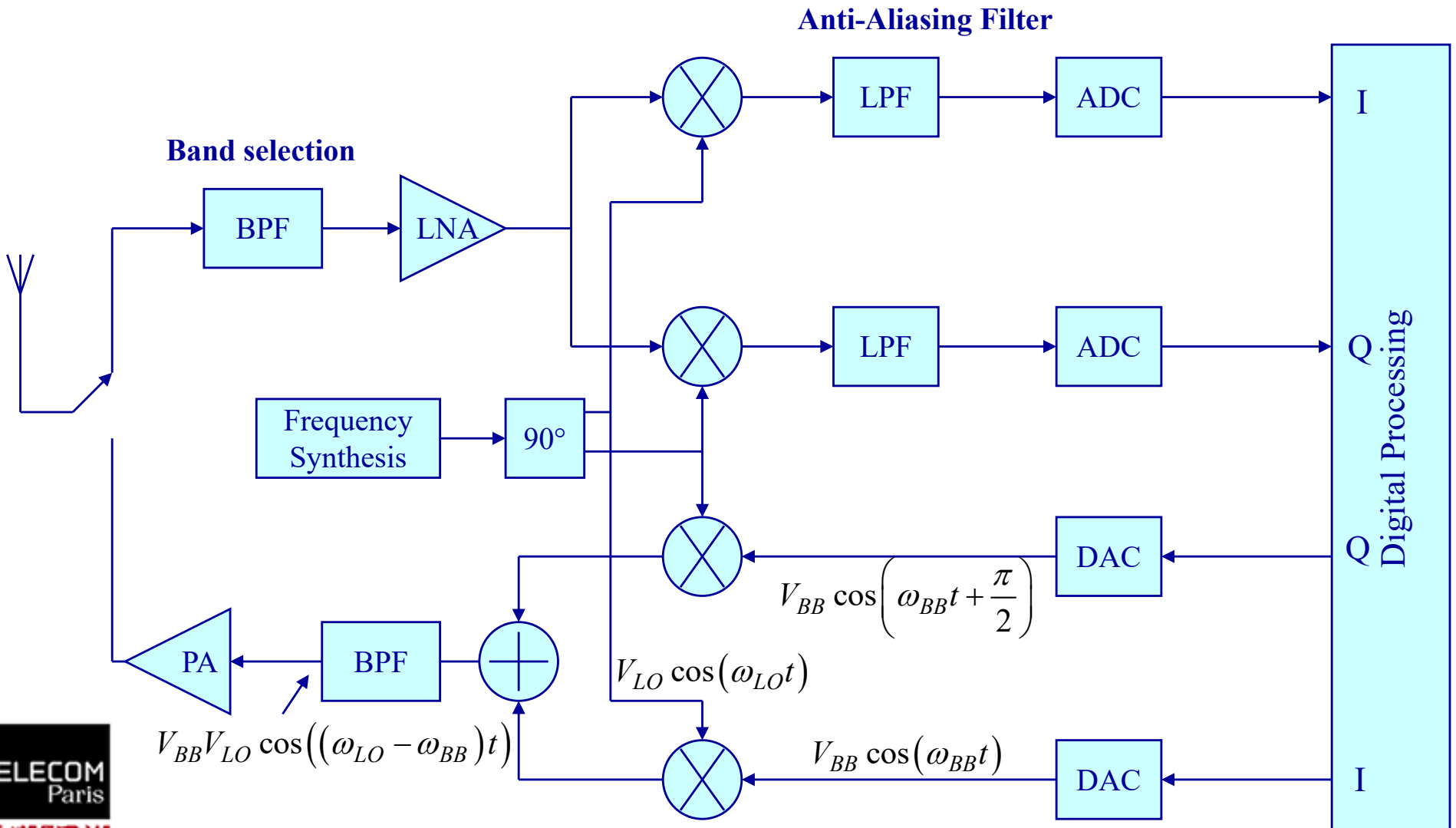
– Military & Defense communications : from 1 to 100 GHz approximately (exact frequency bands and related applications are kept secret !!!)



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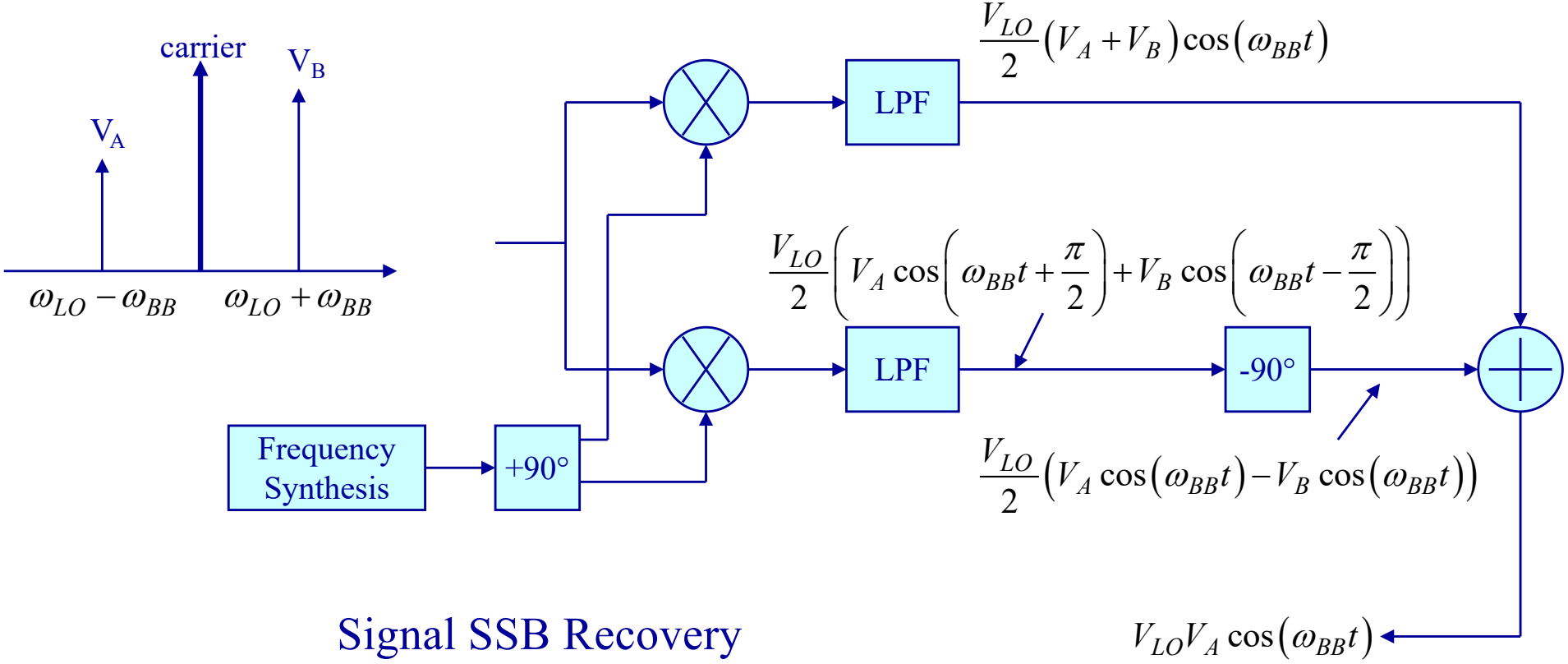
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Transceiver chain



Direct conversion transceiver SSB

Single-Side Band Transceiver



Signal SSB Recovery

RF frequency synthesis: RF oscillator, PLL

$$f_{LO} = f_0 + k\, f_{ch}$$ Chanel selection

Mixer converts signal band around carrier frequency down to DC (baseband)

Key functions

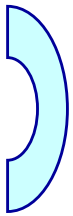
Almost all the functions are implemented in digital signals :

- Coding/decoding
- Modulation/demodulation (amplitude, frequency or phase)
- Pulses shaping (raised cosine filtering)

A few analog functions remain unavoidable :

- LNA, Mixers
- Power amplifiers
- Filters
- ADC & DAC

- RF oscillators
- PLLs
- Frequency synthesizers



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Signal and noise in the receiver

• **Signal-to-Noise Ratio** (SNR) : Power of the wanted signal P_S divided by the power of the noise P_N (and distortion SINAD) in the band of interest B, expressed in dB

$$SNR = 10 \log_{10} (P_S / P_N)$$

• **Noise Figure** (NF) : The internal electrical noise added by the receiver components, expressed in dB

$$NF = 10 \log_{10} (SNR_{input} / SNR_{output})$$

• **Sensitivity** (S_{min}) : weakest RF signal power that can be processed to develop a minimum signal-to-noise ratio for achieving a required bit error rate (BER)

•**Dynamic range** (DR) : ratio between signal max S_{max} and signal min S_{min}

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Standard RF Receiver Sensitivity Formula

- Receiver sensitivity (S_{min}) in dBm is calculated as :

$$S_{min} = -174\,dBm/Hz + 10log_{10}B(Hz) + NF(dB) + SNR_{min}(dB)$$

- -174 dBm/Hz: The thermal noise floor power density at room temperature (290°K) in a 1 Hz bandwidth.
- B: The noise bandwidth of the receiver in Hertz (Hz)
- **Noise Figure** (NF) : The internal electrical noise added by the receiver components, expressed in dB
- SNR_{min} : The minimum signal-to-noise ratio required at the demodulator to reliably decode the data (or achieve a target Bit Error Rate BER)

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Signal integrity in wireless communications

- Signal integrity means signal preservation during communication via the RF transceiver **:**
  - ***Voltage, timing, and shape preservation***
- Frequency synthesizers act as the core local oscillators or sample clocks in RF, radar, and high-speed digital designs
- Signal integrity in systems using frequency synthesizers means **transferring or generating signals without excessive distortion (spurs), phase error, or timing jitter.**

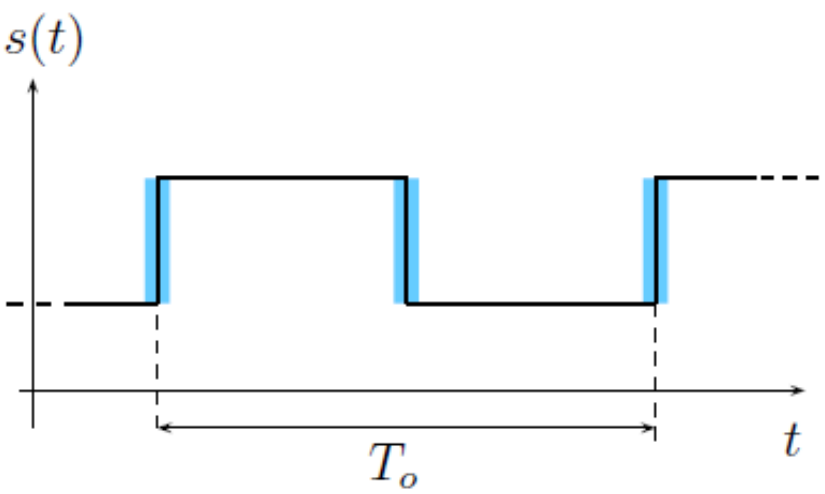
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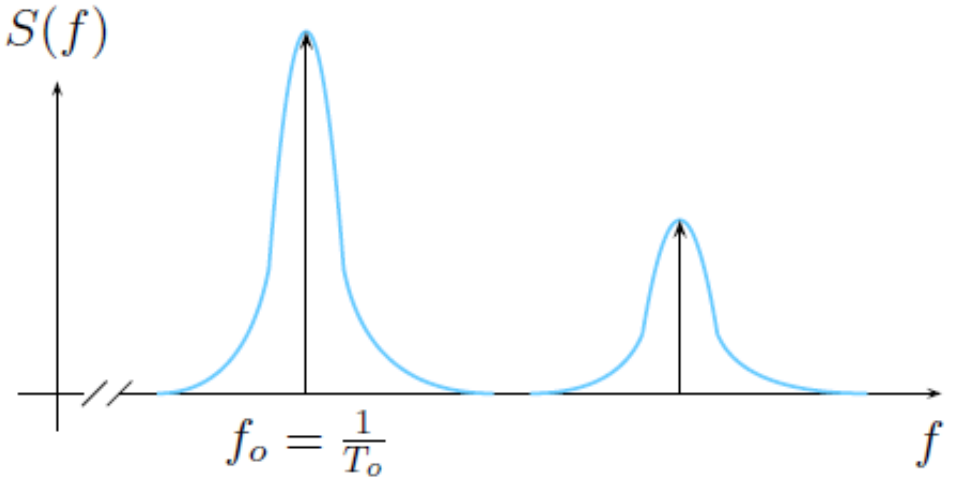
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Phase Noise & Jitter

- Phase noise and jitter are two manifestations of an unique phenomena : random fluctuations of the oscillator period.

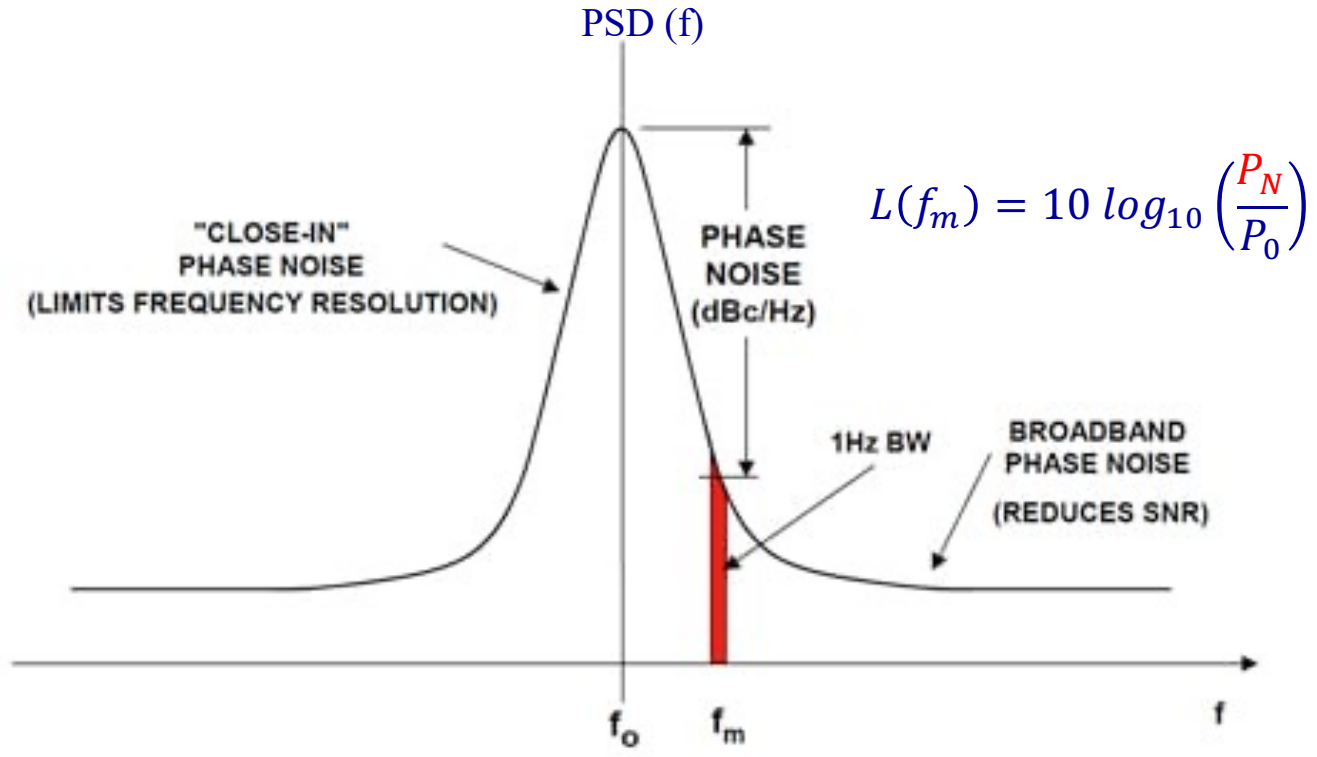
- Phase noise is associated to spectral representation whereas jitter is associated to time representation of these fluctuations





Phase Noise & Jitter

Jitter RMS $$J_{\mathrm{RMS}} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(T_i - T_{\mathrm{moy}})^2} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(\Delta T_i)^2}$$

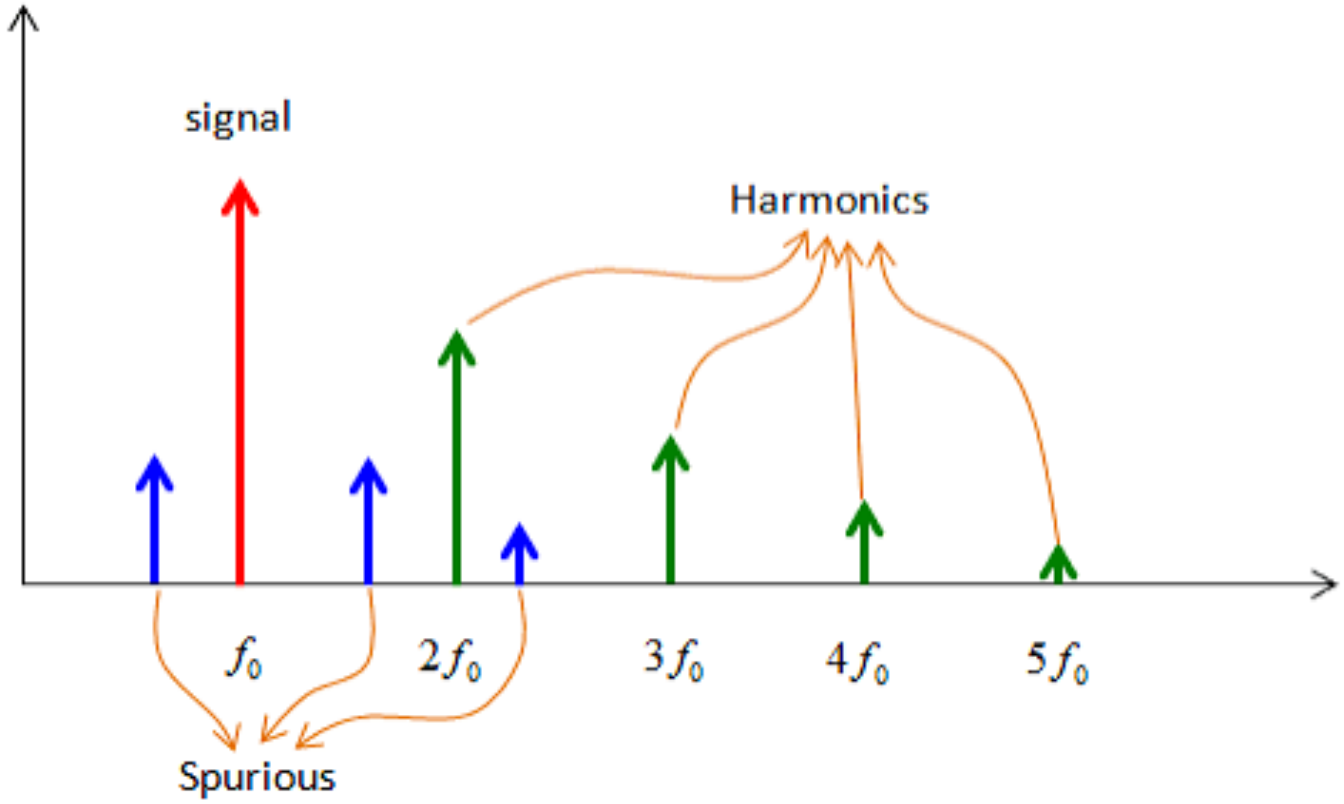


$$L(f_m) = 10\ log_{10}\left(\frac{P_N}{P_0}\right)$$

Main impact : Reciprocal mixing degrade the SNR of the transmission

Spurious Tones ("Spurs") & Harmonics

- Unwanted, distinct frequencies appearing in the output spectrum of a frequency synthesizer alongside the desired carrier signal



Main impact : can severely degrade receiver selectivity and sensitivity

Spurious Tones ("Spurs") & Harmonics

- **Selectivity** : receiver selectivity is a radio receiver's ability to pick up a desired frequency or channel while blocking out unwanted signals on nearby or adjacent frequencies

- **Impact of Spurious Tones & Harmonics**

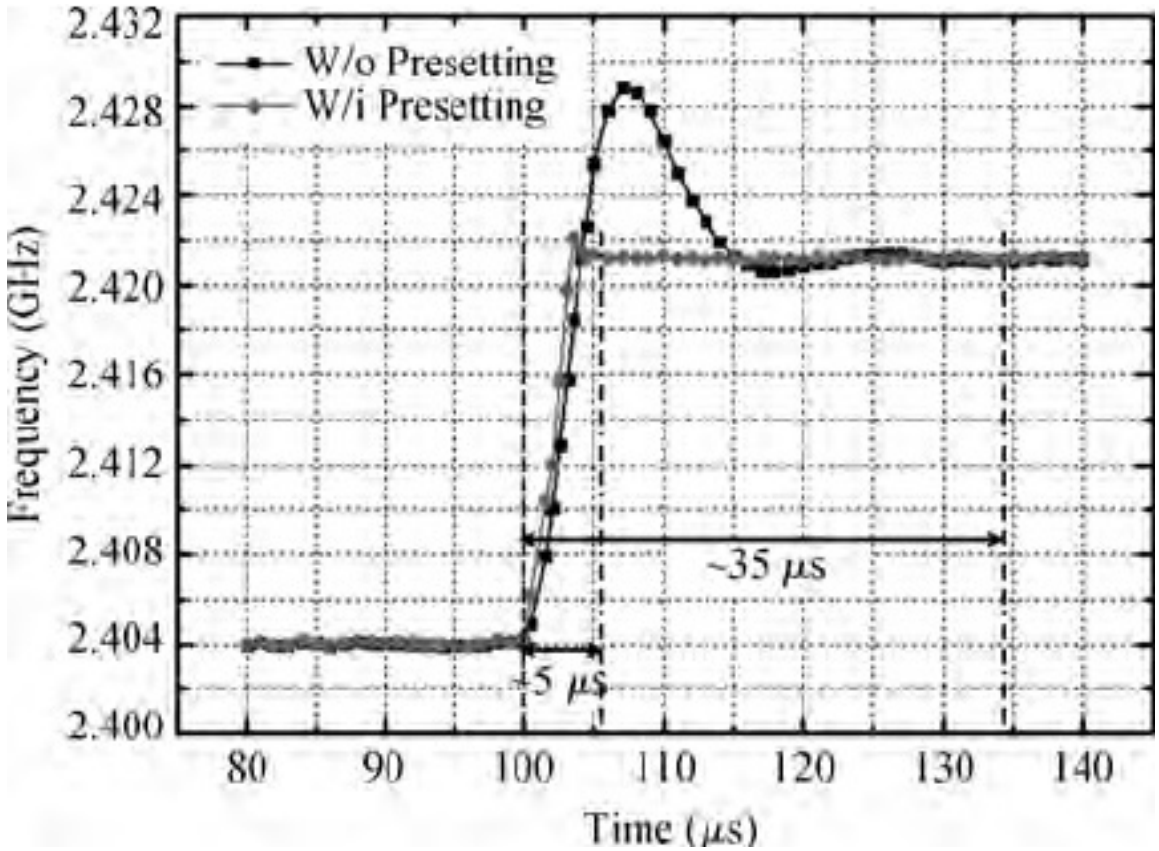
- **Transmitters:** Spurs can cause emissions to violate regulatory spectral masks and create out-of-band interference.
- **Receivers:** Spurs can down-convert strong blockers or interferers directly into the desired channel signal, degrading receiver sensitivity and making the data irretrievable.
- **System Metrics:** High spur levels degrade the Bit Error Rate (BER).

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Switching Speed & Settling Time

- **Switching speed** (or Lock Time) and **settling time** are critical performance metrics that define how fast a frequency synthesizer can jump from one frequency f_1 to another f_2 and stabilize within an acceptable error band.



Switching Speed & Settling Time

- In modern RF systems—such as fast frequency-hopping radar, 5G/6G time-division duplexing (TDD), and multi-band transceivers—**these metrics dictate how much data can be transmitted and how efficiently the spectrum is used**.

- **Main Determining Factors :**
  - ***For the switching speed : Architecture, loop bandwidth, register programming time.***
  - ***For the settling time : Loop filter design, damping factor, phase margin***

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Summary

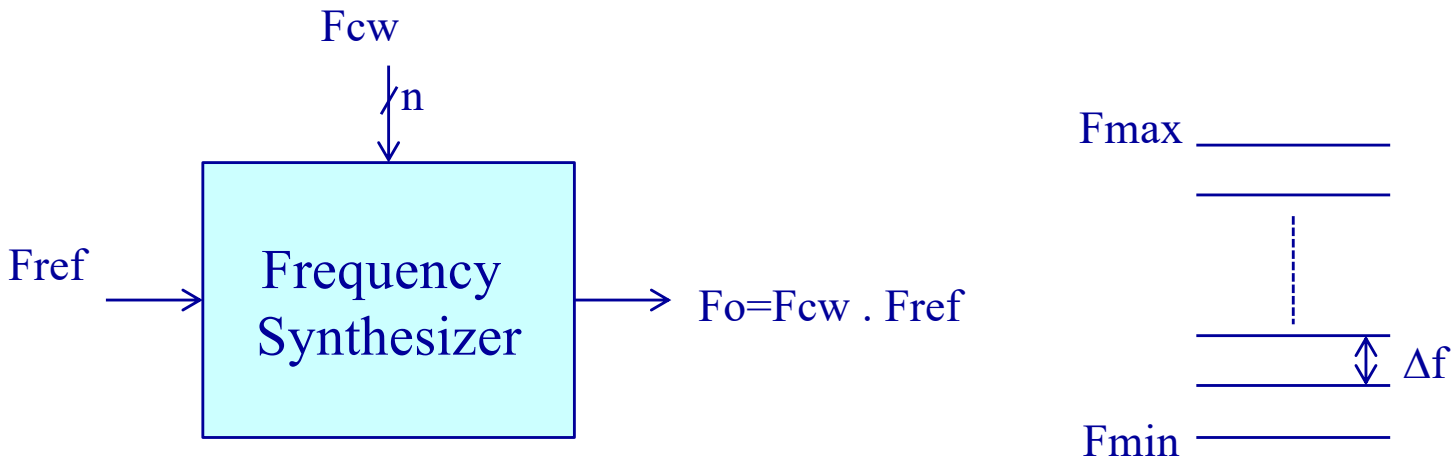
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Frequency synthesizer

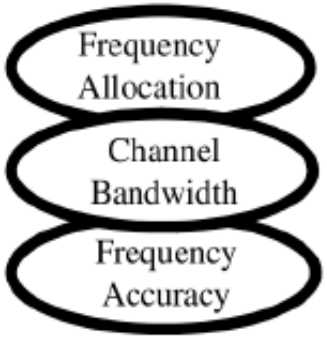
The “black box” view of a frequency synthesizer is a block getting a very stable reference frequency (usually provided by quartz oscillator) and delivering a set of frequencies between F_{min} and F_{max} with a resolution of Δf :



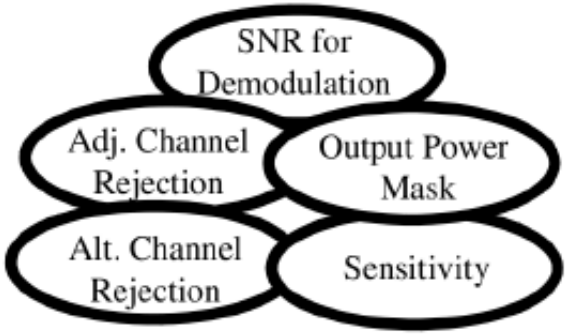
The frequency range [F_{min}, F_{max}] and the resolution Δf are synthesizer fundamental specifications which depend on the application.

Main specifications

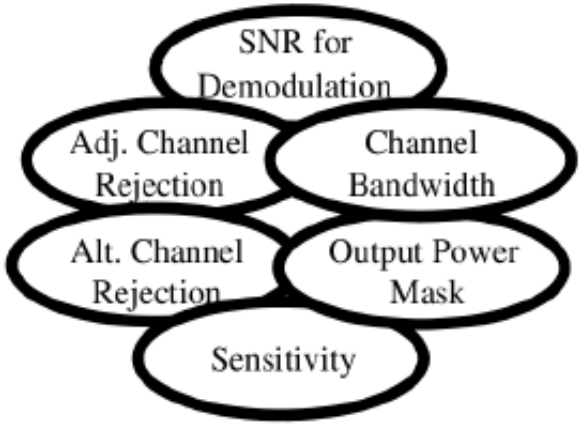
- Frequency range
- Resolution
- Accuracy
- Settling time
- Reference frequency
- Spurs
- Power consumption
- Temperature stability
- Phase noise



Frequency Synthesis



Spur Rejection



Phase Noise



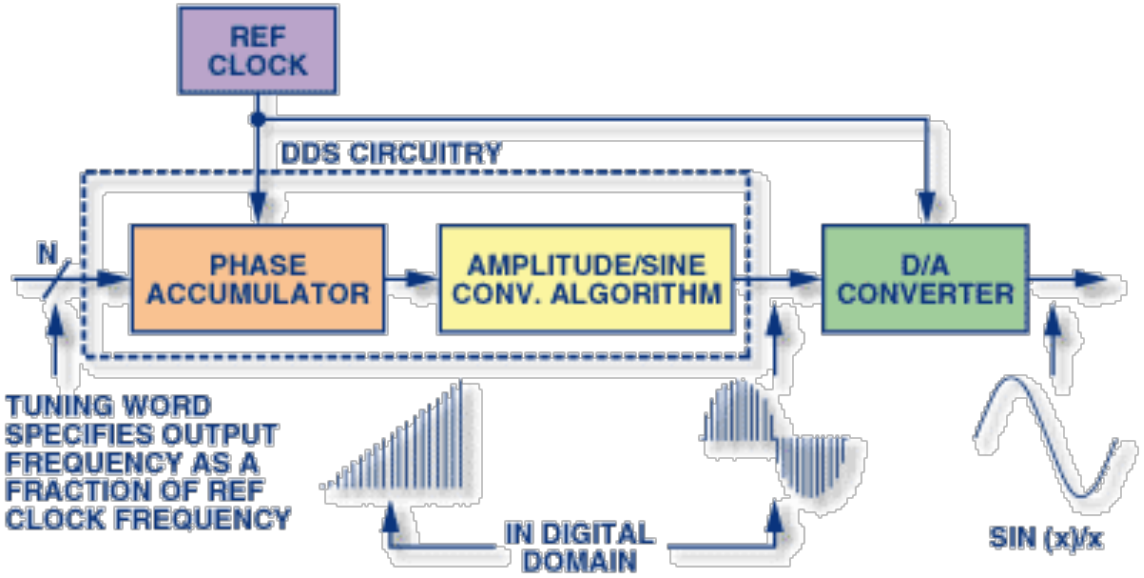
Settling Time

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Different types of Frequency synthesizers

- **Direct Digital Synthesis (DDS)**
  - *to generate highly precise analog waveforms (such as sine, square, and triangular waves or modulated signals) from a single, fixed-frequency digital reference clock.*



++ : Fast Switching Speed
Digital programmability

-- : Phase truncation, low-level spurious noise

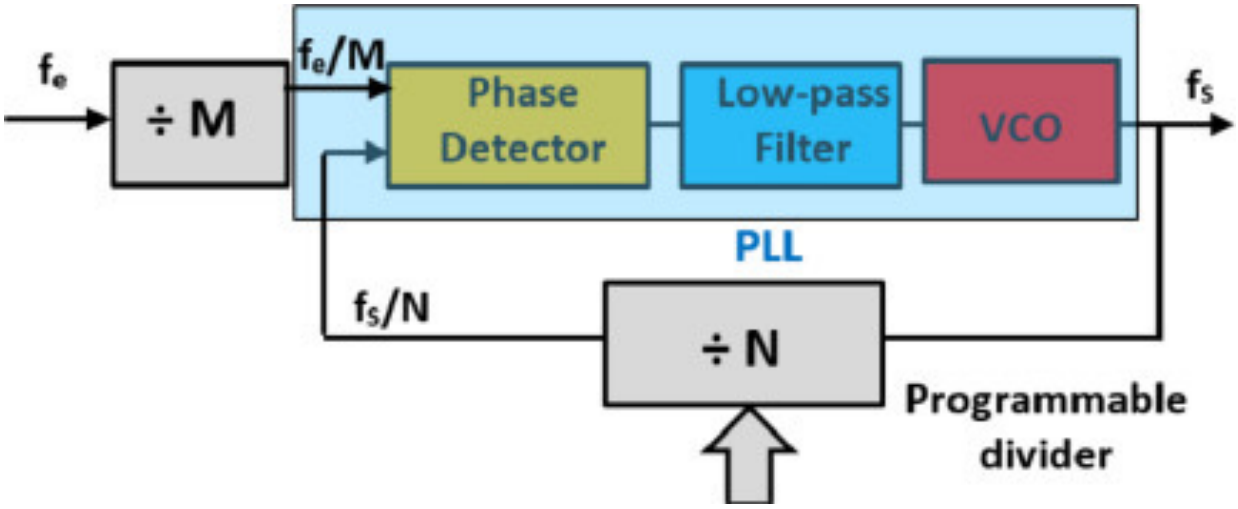
- *Main limitation : lower maximum output frequencies compared to analog RF Synthesis.*

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Different types of Frequency synthesizers

- **Indirect Frequency Synthesis (PLL)**
  - ***to generate a wide range of stable output frequencies from a single, high-precision reference oscillator by using a closed-loop feedback system.***



++ : High Spurious Rejection,
Digital programmability,
Cost & Integration Efficiency

-- : Slower Switching Speed

- ***Main limitation : Phase noise is mainly linked to the VCO.***

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Direct vs. Indirect Synthesis (DDS vs. PLL)

Metric	Direct Digital Synthesis (DDS)	Indirect Synthesis (PLL)
Maximum Frequency	Lower (limited by DAC speed and Nyquist limits).	**Extremely High** (VCOs can reach tens of GHz comfortably).
Tuning / Lock Speed	**Near-Instantaneous** (switches clock-to-clock).	Slower (limited by the analog settling time of the loop filter).
Phase Noise	Generally higher far-from-carrier noise floor.	**Excellent close-in phase noise** near the carrier frequency.
Frequency Resolution	Sub-Hertz out of the box (controlled by accumulator bit-width).	Coarse in basic Integer-N; exceptionally fine in advanced Fractional-N.
Signal Purity	Suffer from discrete, numeric phase-truncation spurs.	High spectral purity; clean harmonics if properly filtered.

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Summary

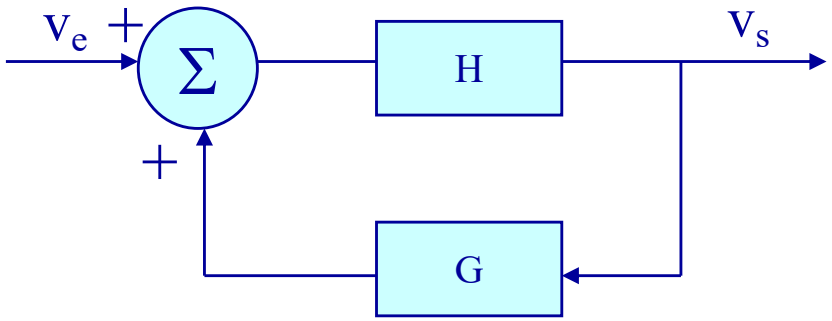
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RF oscillators - Introduction

An oscillator must provide a self-sustaining periodic signal

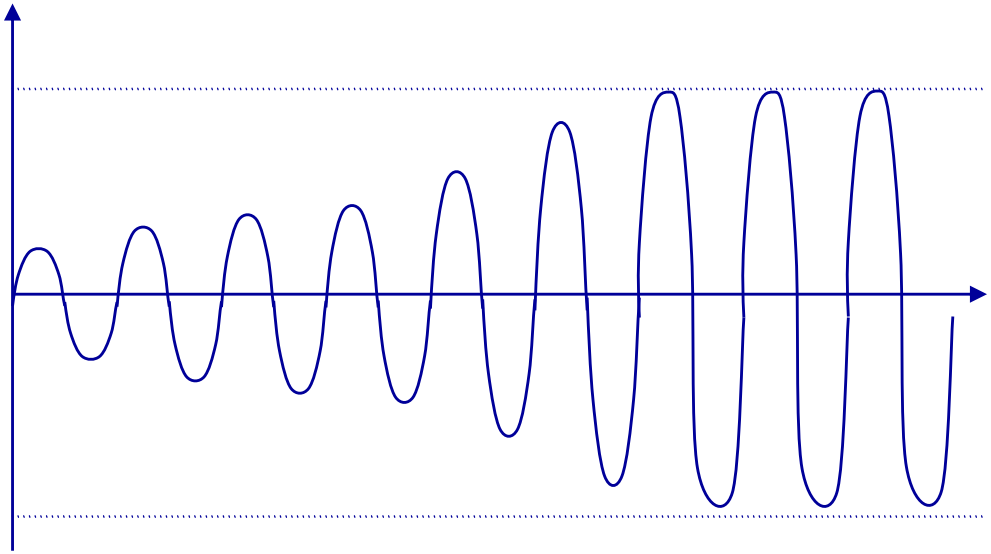


Positive feedback system

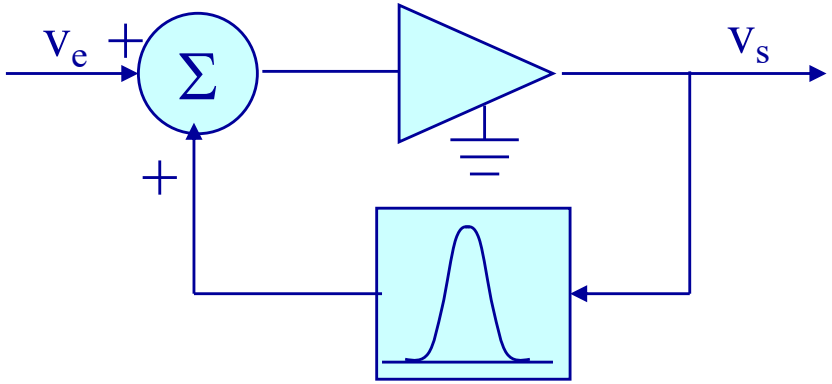
$$V_s = \frac{H(j\omega)}{1 - G(j\omega)H(j\omega)} V_e$$

Barkhausen criterion

$$\begin{cases} |G(j\omega_0)||H(j\omega_0)| = 1 \\ \arg\{G(j\omega_0)H(j\omega_0)\} = 0 \end{cases}$$

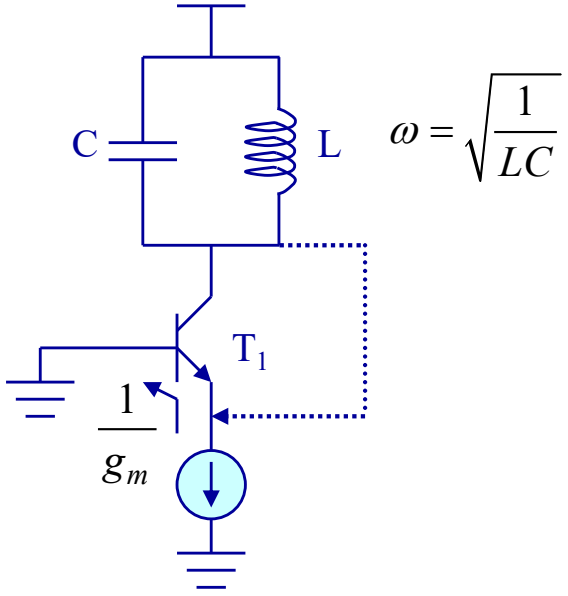


RF oscillators – Frequency selection

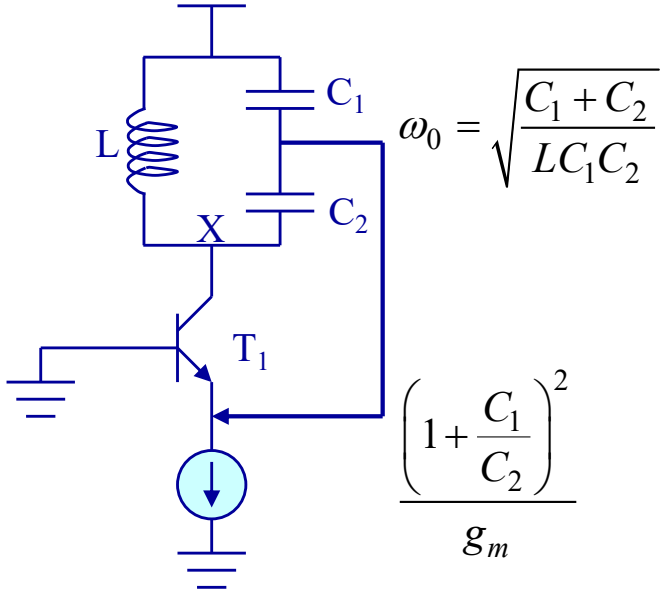


Frequency selective network or resonator

The system oscillations frequency is determined by the characteristics of the selective circuit.

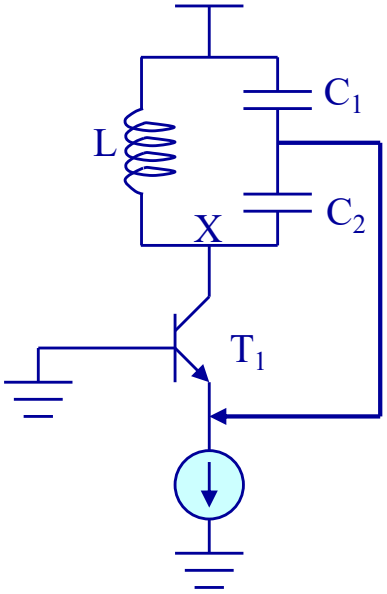


Direct return from collector to emitter



Colpitts oscillator

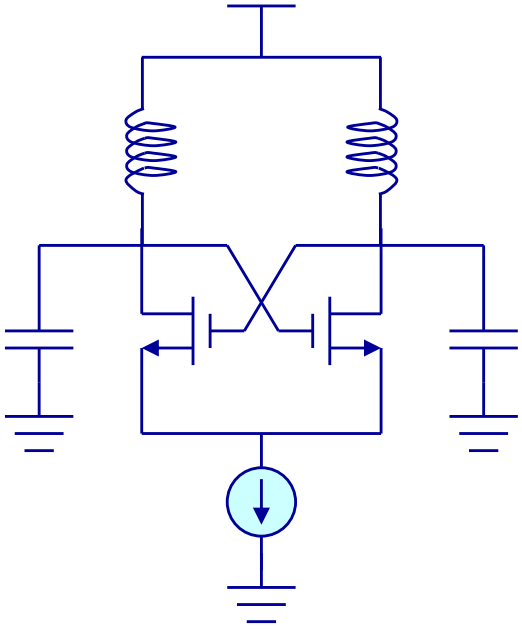
RF oscillators – LC Architecture



Colpitts oscillator

Pros : High quality factor
One single inductor

Cons : Large ratio C_1/C_2
One terminal output

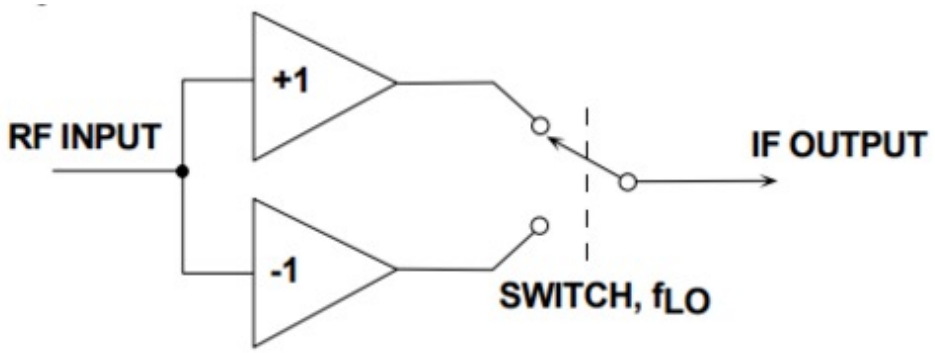


CMOS differential architecture

Pros : High quality factor
Differential output

Cons : Matching of the two LC cells

RF oscillators – Output waveforms

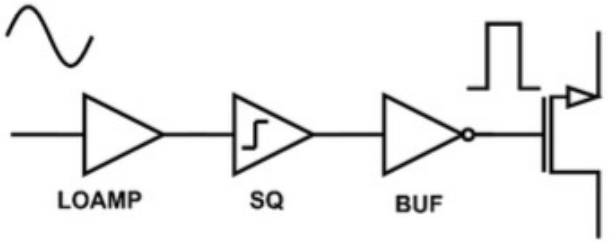


An ideal Switching Mixer

Mixer good behavior is favored if the waveform of the local oscillator (LO) exhibits abrupt transitions and if the duty cycle is equal to 50%

•**Sine Wave:** Common in high-frequency RF and microwave synthesizers (typically above 1 GHz to several gigahertz) where LC tank resonators produce smooth sinusoidal oscillation.

•**Square Wave / Pulse Wave:** Produced when the VCO output passes through an internal or external digital frequency divider (N-counter) or a clock buffer/limiter (such as LVCMOS drivers).



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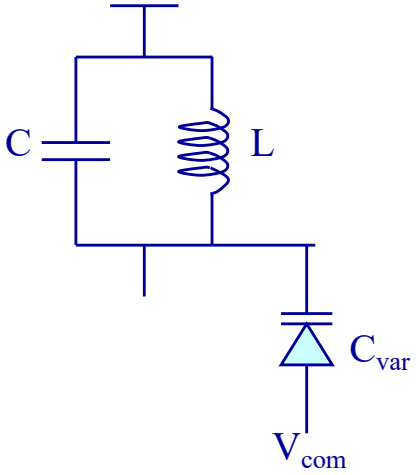
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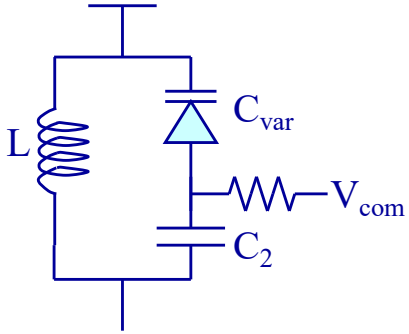
Voltage Controlled RF oscillators (VCO)

- Need to obtain an adjustable frequency RF oscillation for channel selection :

$$f_{LO} = f_0 + k\, f_{ch}$$

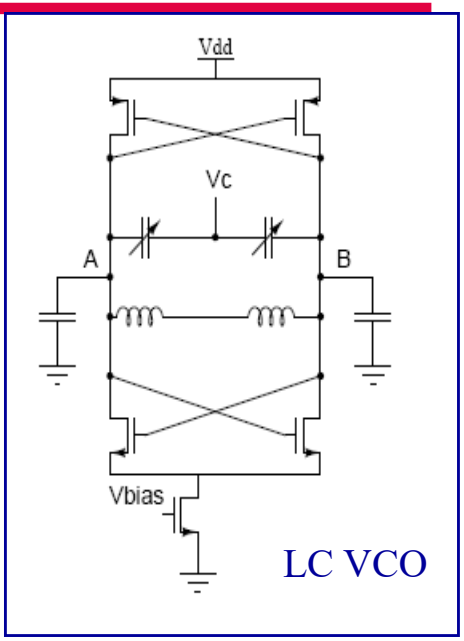
- Frequency value controlled by a voltage





$$C_{\text{var}}(V_{com}) = \frac{C_0}{\left(1 - \frac{V_{com}}{V_{diff}}\right)^{\frac{1}{2}}}$$

Use of a varicap diode in the LC cell



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Voltage Controlled RF oscillators (VCO)

- VCO mathematical model

$$\omega_{LO} = \omega_{FR} + K_{VCO} V_{com} = \frac{d\Phi}{dt}$$

$$X(t) = V_{LO} \cos(\Phi) = V_{LO} \cos\left(\omega_{FR} t + K_{VCO} \int V_{com} dt\right)$$

- If the control voltage is constant, the frequency is shifted by $K_{VCO}V_{com}$

$$V_{com} = V_0$$

$$X(t) = V_{LO} \cos\left(\left(\omega_{FR} + K_{VCO} V_0\right) t + \phi_0\right)$$

- The VCO is a frequency modulator

$$V_{com} = V_m \cos(\omega_m t)$$

$$X(t) = V_{LO} \cos\left(\omega_{FR} t + \frac{K_{VCO}}{\omega_m} V_m \sin(\omega_m t)\right)$$

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RF oscillators – Phase noise

- Origin : internal noise of components constituting the oscillator
  example : amplifier thermal noise and flicker noise
  (use of a single transistor to minimize)

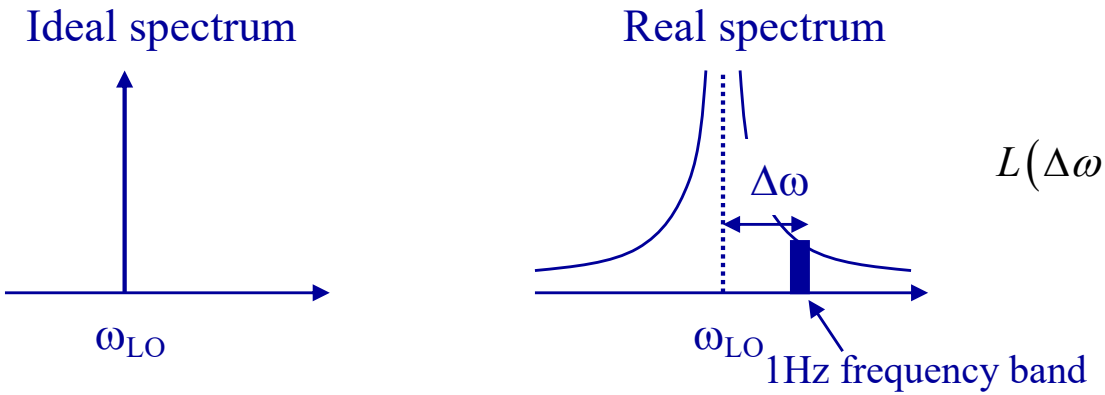
- Main effect : Random deviation of output wave frequency

$$X(t) = V_{LO}\cos\left(\omega_{LO}t + \Phi_n(t)\right)$$

$$si \quad \left|\Phi_n(t)\right| << 1 \quad , \quad X(t) \approx V_{LO}\left\{\cos\left(\omega_{LO}t\right) - \Phi_n(t)\sin\left(\omega_{LO}t\right)\right\}$$

$\Phi_n(t)$: phase noise

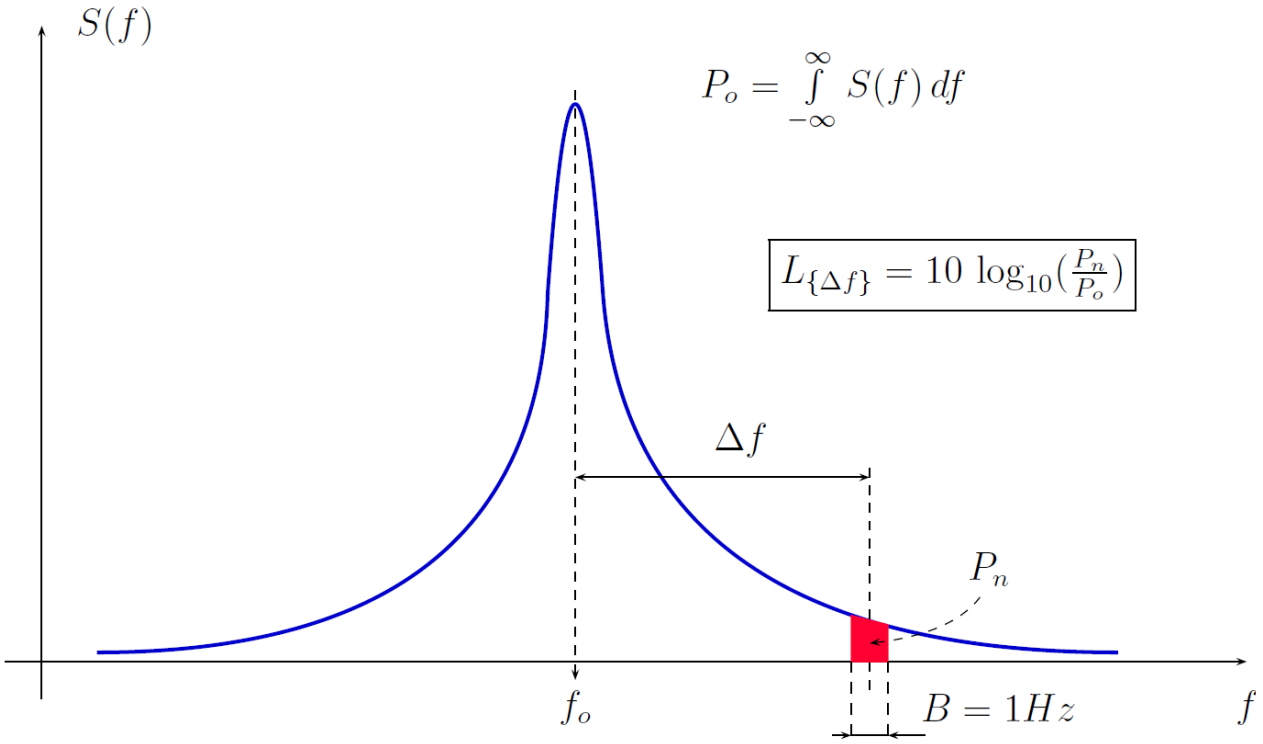
- Frequency domain characterization for RF applications :



$$L(\Delta\omega) = 10\log\left(\frac{P_n}{P_{LO}}\right) \quad [dBc/Hz]$$

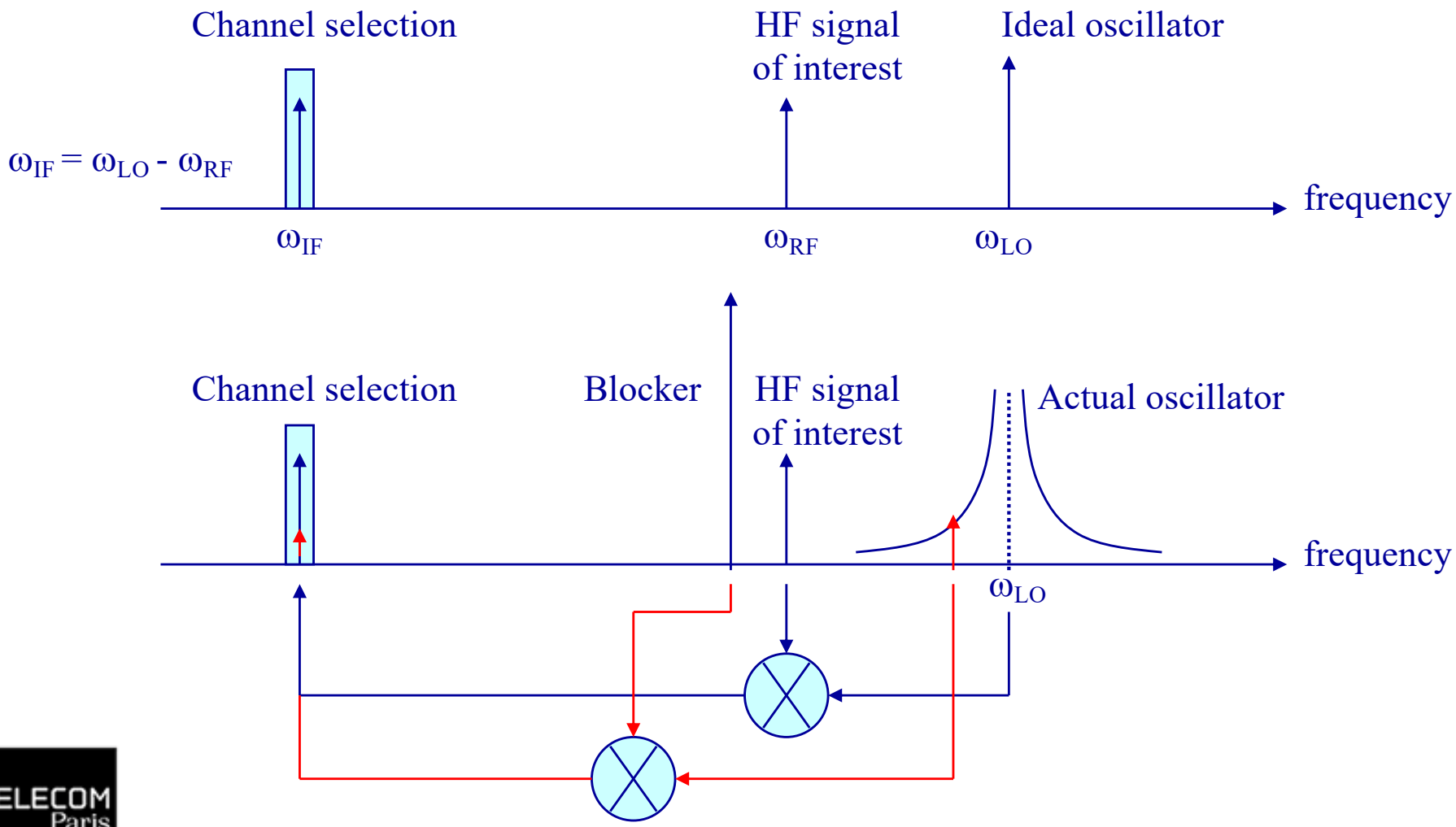
Spectral characterization

- Thus, because of the different noise sources (thermal, 1/f…) the Power Spectral Density (PSD) spreads around f_0



Example (DECT standard 1 880-1 900 MHz) : -97dBc/Hz @ 1,8 MHz

Phase noise – Reciprocal mixing

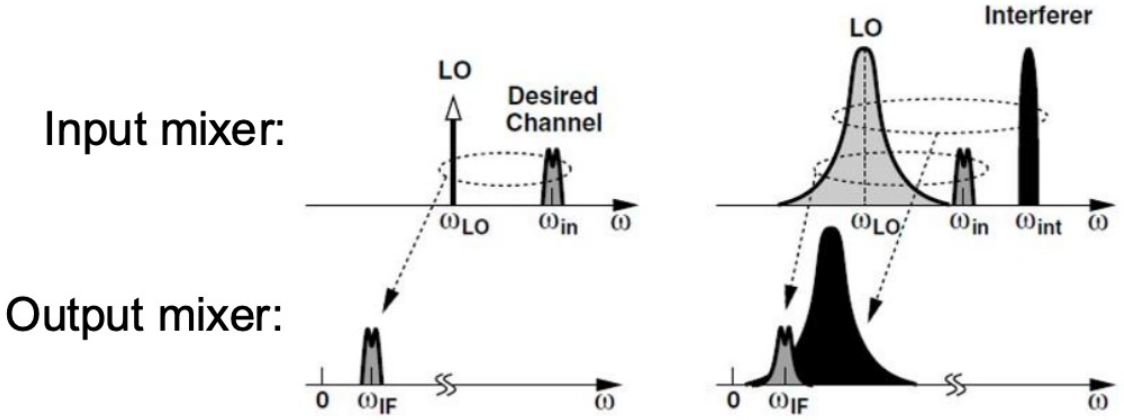


Addition of noise during down-conversion to reception

Phase noise – Reciprocal mixing

$$P_{reciprocal} = P_{blocker} + L(\Delta f) + 10\log(BW)$$ in dBc

Where $L(\Delta f)$ is the phase noise power at the offset frequency from the LO frequency

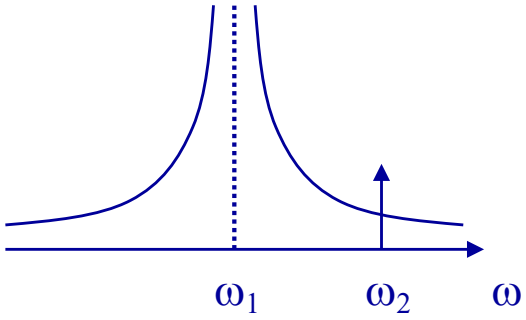


The reciprocal mixing increases the NF at the output of the mixer, which then reduces the sensitivity of the receiver. This increase in noise figure is so called Degradation of Noise Figure or DNF

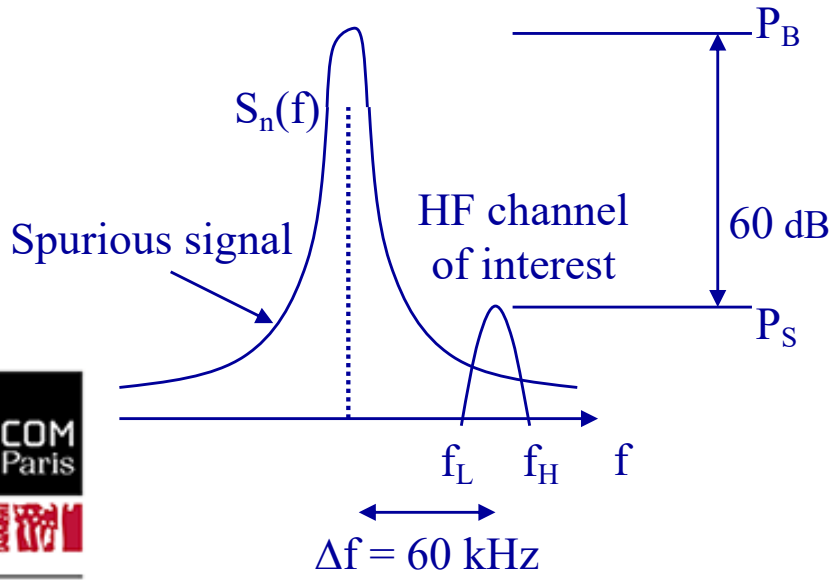
Example (UWB standard) : the DNF due to Wi-Fi signals with power of -23.5 dBm should remain lower than 1.7 dB

Phase noise – Specification example

Real spectrum of the transmitter



Adding noise during up-conversion to transmission



Calculation of a phase noise specification for the RF oscillator :

Bandwidth of interest : $f_H - f_L = 30$ kHz
Assumption : $L(\Delta f)$ is constant in this band

$$L(\Delta f) = L_0 \text{ [dBc/Hz]}$$

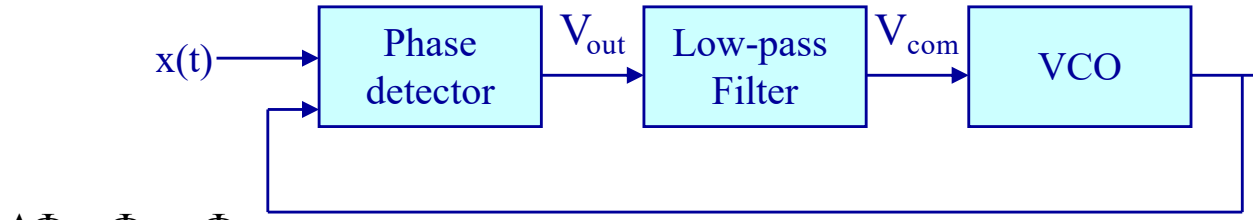
What is the maximum value of L_0 that guarantees an SNR in the channel of interest greater than 15 dB?

?

Summary

- Digital Transceiver RF Front-end
- Signal Integrity
- Frequency Synthesizers
- RF oscillators
- **PLLs**
- Indirect frequency synthesis

PLL – Presentation



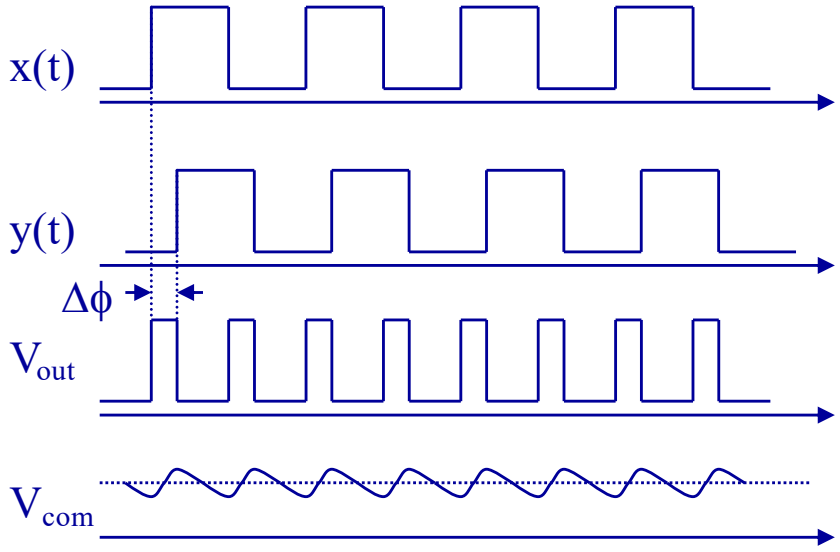
$$\Delta\Phi = \Phi_x - \Phi_y$$

$$V_{com} = K_{DP}\Delta\Phi$$

$$y(t) = V_{LO}\cos\left(\omega_{FR}t + \Phi_y\right)$$

$$\Phi_y = K_{VCO}\int V_{com}dt$$

Basic Phase Locked Loop



PLL waveforms

The loop is locked when $\Delta\Phi$ is constant, which corresponds to the equality of the input and output frequencies.

$$\omega_y = \omega_{FR} + K_{VCO}V_{com} = \omega_x$$

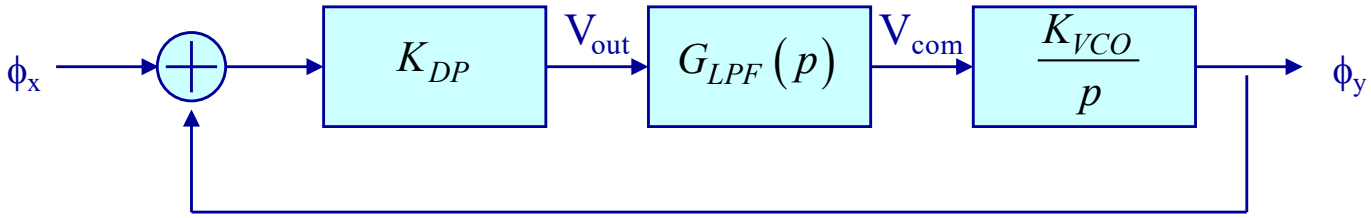
$$\Delta\Phi = \frac{V_{com}}{K_{DP}} = \frac{\omega_x - \omega_{FR}}{K_{DP}\cdot K_{VCO}}$$

The frequency are exactly equal !

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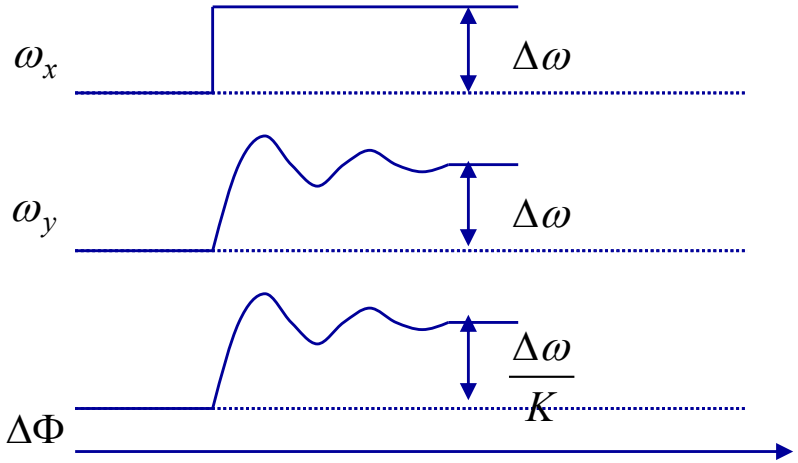
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PLL – Dynamic behavior



Closed loop transfer function: $H(p) = \dfrac{\Phi_y(p)}{\Phi_x(p)} = \dfrac{K\, G_{LPF}(p)}{p + K\, G_{LPF}(p)}$ *avec* $K = K_{DP} K_{VCO}$

with first order low-pass filter: $G_{LPF}(p) = \dfrac{1}{1 + \dfrac{p}{\omega_{LPF}}}$, we obtain a classical second order system:



$$H(p) = \frac{\omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}$$

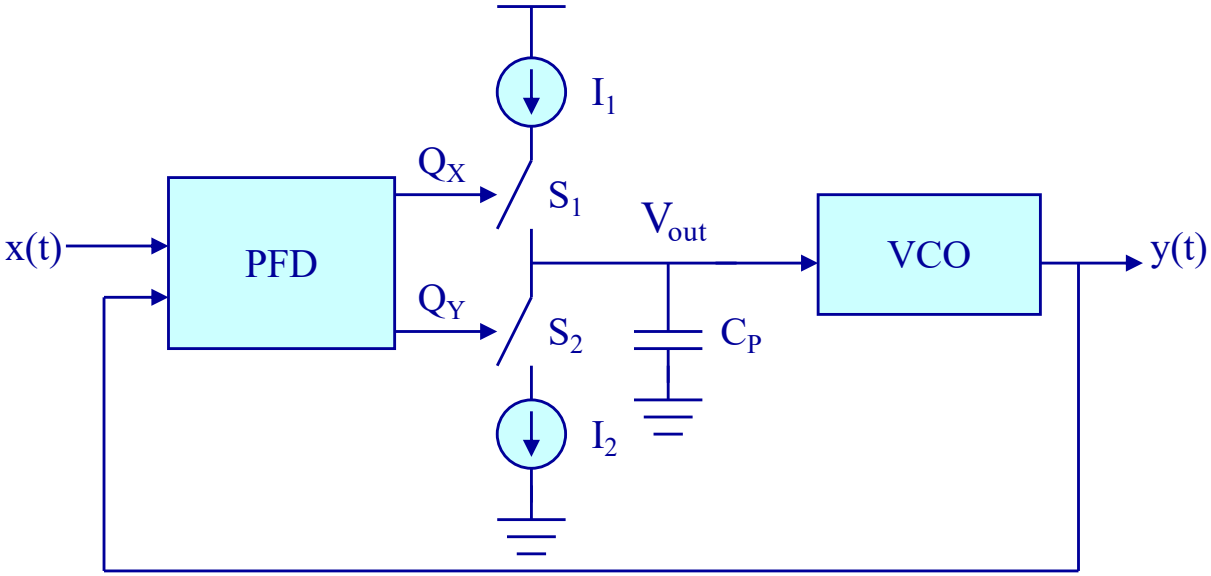
avec $\omega_n = \sqrt{\omega_{LPF} K}$

et $\zeta = \dfrac{1}{2}\sqrt{\dfrac{\omega_{LPF}}{K}}$

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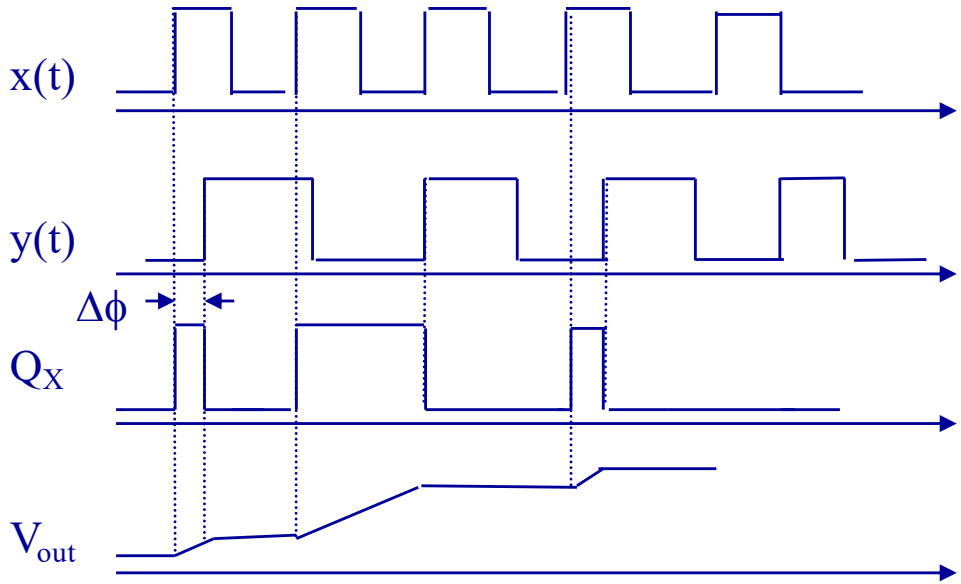
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Charge Pump PLL



Architecture with 3-state phase/frequency detector and charge pump circuit

$$I_1 = I_2 = I$$



Waveforms in CPPLL with $\omega_x > \omega_y$ in closed loop :

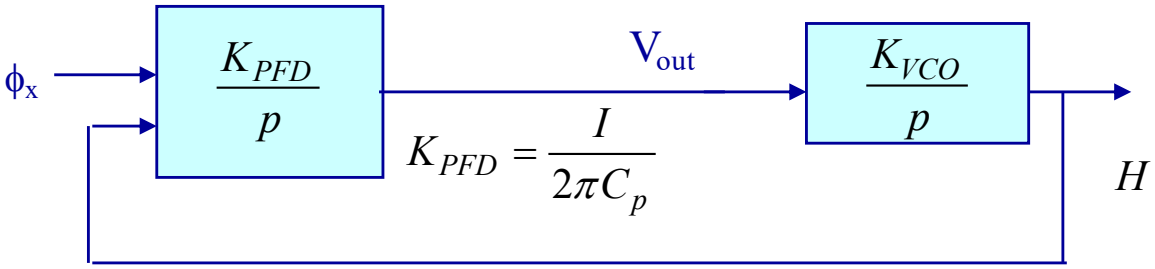
$$V_{out} \quad cons\tan t$$
$$\omega_y = \omega_{FR} + K_{VCO} V_{out} = \omega_x$$
$$\Delta\Phi = \Phi_x - \Phi_y = 0$$
$$Q_X = Q_Y = 0$$

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Charge Pump PLL

Assuming that the bandwidth of the loop is much lower than the input frequency:



$$K_{PFD} = \frac{I}{2\pi C_p}$$

$$H(p) = \frac{\Phi_y(p)}{\Phi_x(p)} = \frac{K}{p^2 + K} \quad avec \quad K = K_{PFD} K_{VCO}$$

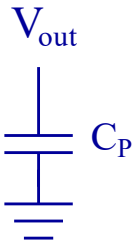
Main difference : two poles at zero in open loop

Pros :

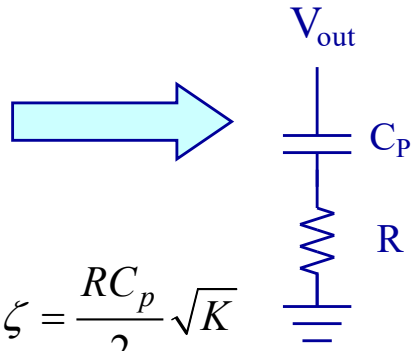
- Maximum extension of the capture range,
- Increase of the locking speed,
- Zero static phase error (if ideal circuits).

Cons :

- Instability issue

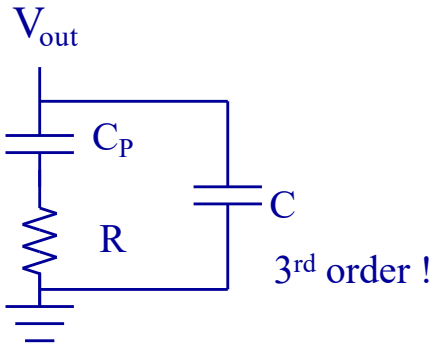


$\zeta = 0$



$$\zeta = \frac{RC_p}{2}\sqrt{K}$$

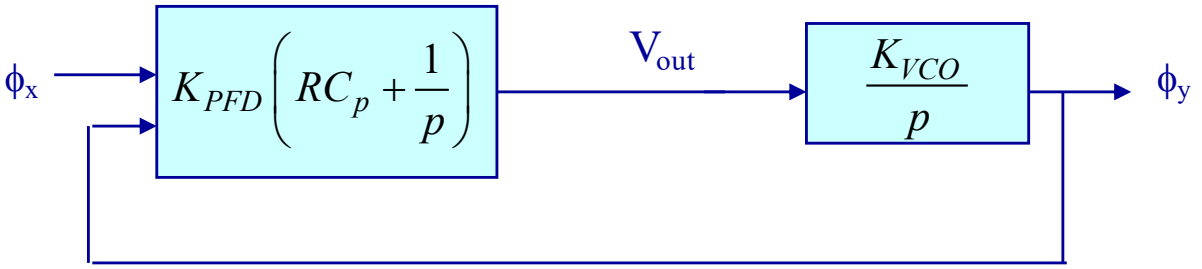
'ripple' ± 2RI



3rd order !

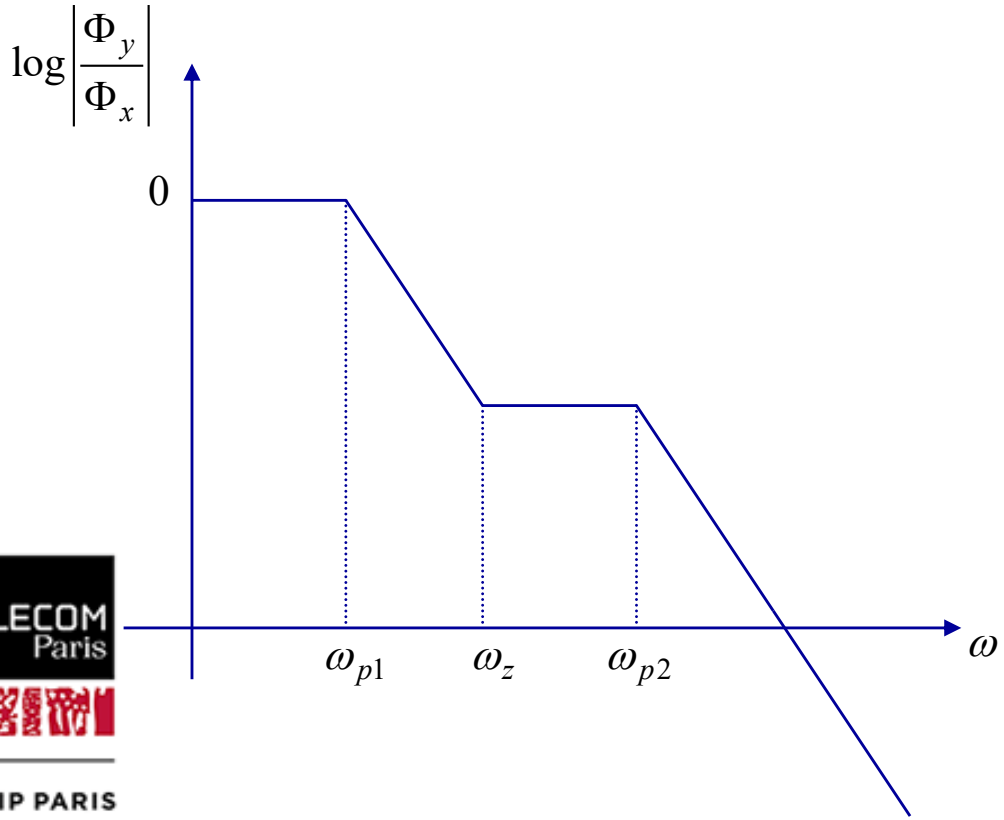
CPPLL – Input phase noise filtering

Transfer function of a second-order CPPLL with a stabilization zero :



$$H(p)=\frac{\Phi_y(p)}{\Phi_x(p)}=\frac{\omega_n^2\left(1+p/\omega_z\right)}{p^2+2\zeta\omega_n p+\omega_n^2}$$

$$avec\ \begin{cases}\omega_n^2=K=K_{PFD}K_{VCO}\\ \omega_z=1/RC_p\end{cases}$$



$$\Phi_x=\phi_0+\Phi_n(t)$$
$$\Phi_y=\phi_0+\Phi_{out}(t)$$

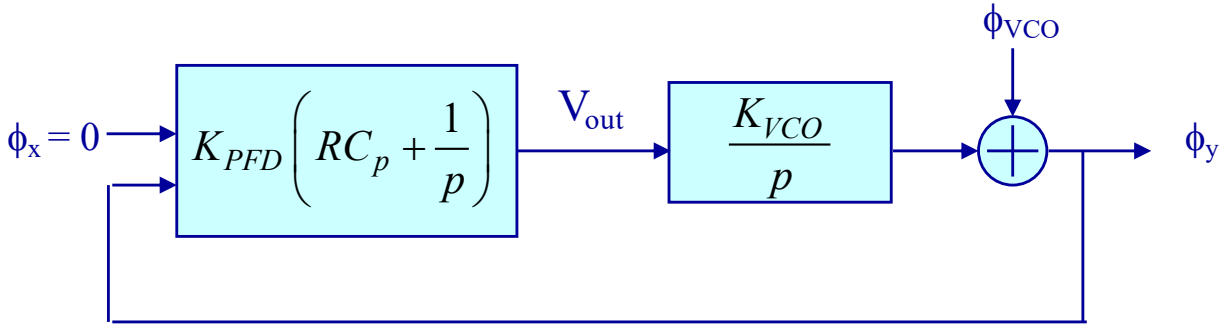
$\Phi_n(t)$: phase noise

- Slow variations of the phase noise are reproduced at the output.
- HF noise is eliminated at the output.

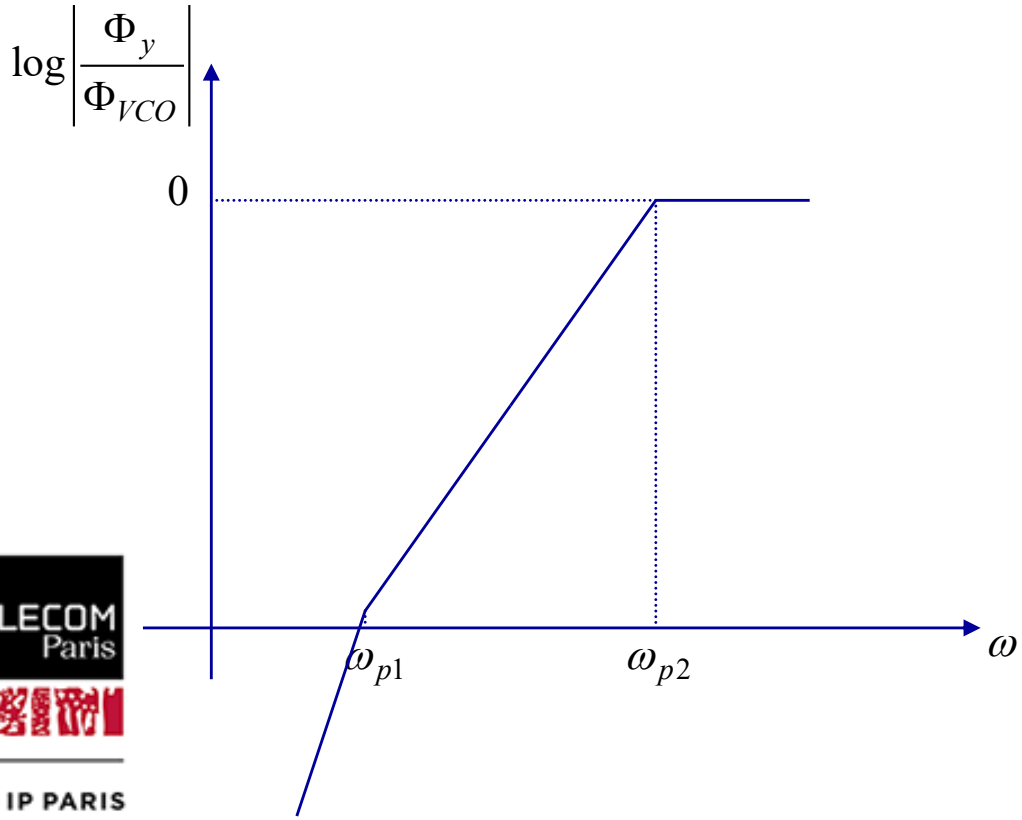
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CPPLL – VCO phase noise filtering



$$\frac{\Phi_y(p)}{\Phi_{VCO}(p)} = \frac{p^2}{p^2 + 2\zeta\omega_n p + \omega_n^2}$$



$\Phi_{VCO} = \Phi_n(t)$

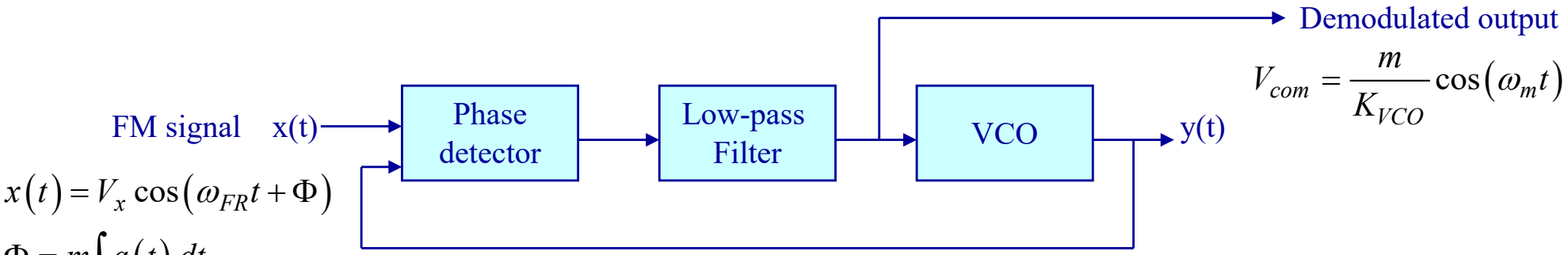
$\Phi_y = \Phi_{out}(t)$

$\Phi_n(t)$: phase noise

- The transfer function is a high-pass filtering
- An increase in the bandwidth of the PLL decreases the phase noise of the VCO

PLL – Applications

RF signal demodulation



$$x(t) = V_x \cos(\omega_{FR} t + \Phi)$$

$$\Phi = m \int a(t)\, dt$$

$$a(t) = \cos(\omega_m t)$$

$$x(t) = V_x \cos\left(\omega_{FR} t + \frac{m}{\omega_m} \sin(\omega_m t)\right)$$

The frequency are exactly equal :

$$\omega_y = \omega_x$$

$$\omega_{FR} + K_{VCO} V_{com} = \omega_{FR} + m \cos(\omega_m t)$$

Important: Loop bandwidth large enough !

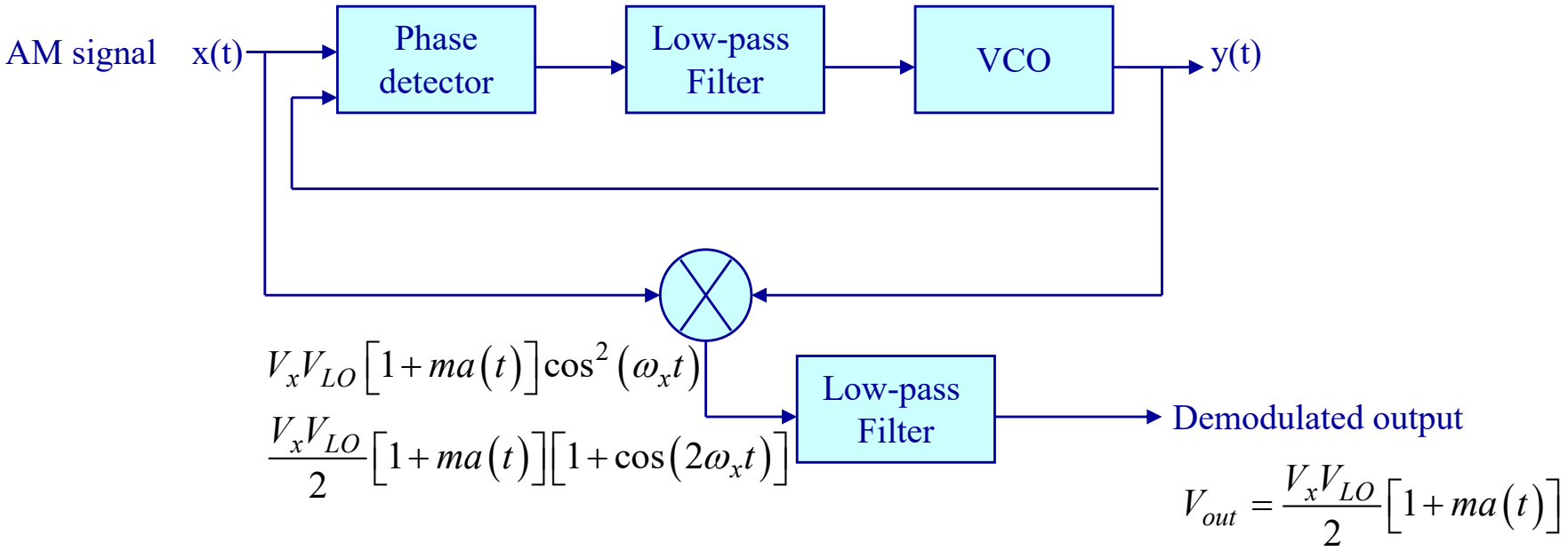
Phase-locked loop for FM demodulator

PLL – Applications

RF signal demodulation

$x(t) = V_x\left[1 + ma(t)\right]\cos(\omega_x t)$

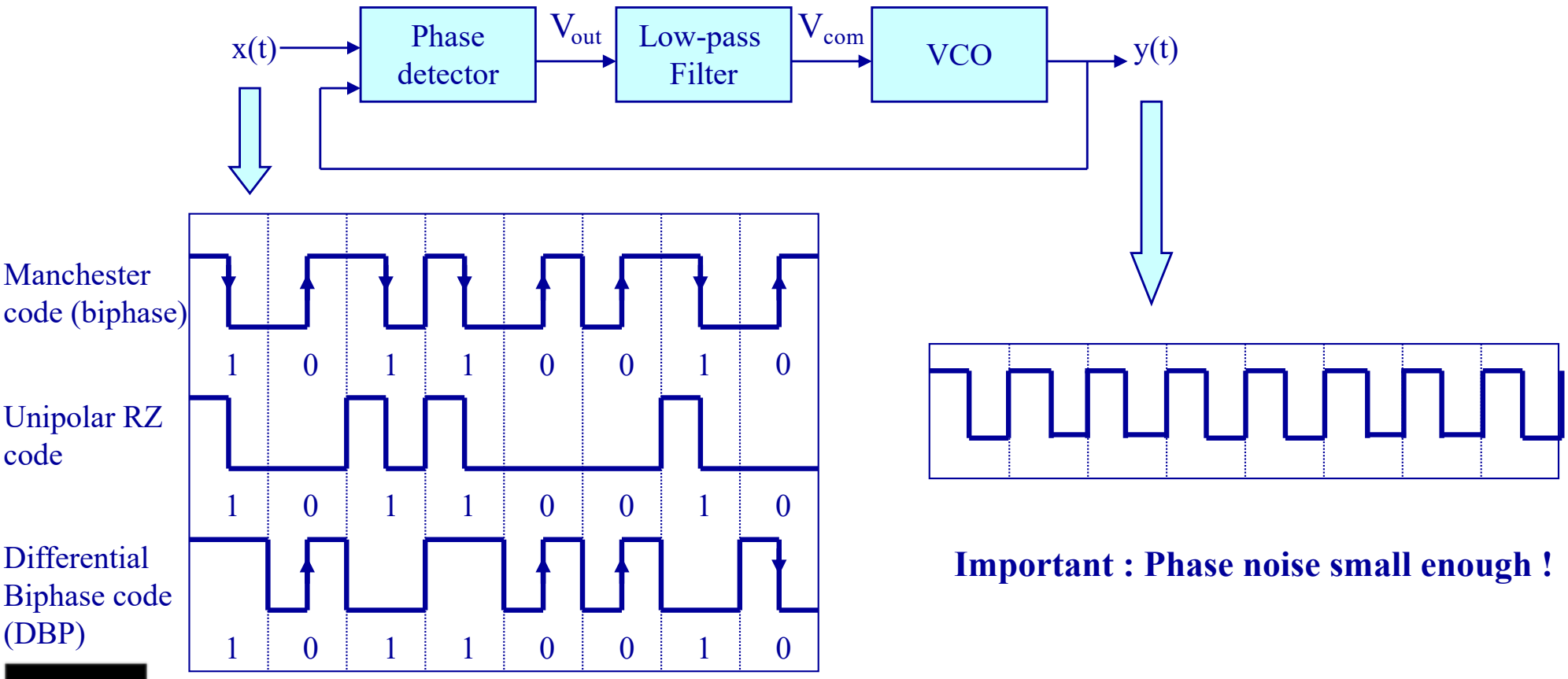
$y(t) = V_{LO}\cos(\omega_x t)$



Phase-locked loop for AM coherent demodulator

PLL – Applications

Clock recovery



Important : Phase noise small enough !

Phase-locked loop for clock recovery from an encoded signal

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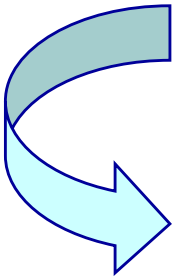
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PLL - Conclusion

Phase locked loops are key elements in digital communications systems. Their design and optimization are complex (trade-off between speed, precision, stability).

Main features are :

- **Locking and Capture Ranges**
- **Agility (locking speed)**
- **Phase noise**
- **Bandwidth**
- **Settling time**



Major application for the RF front end

RF frequency synthesis : RF oscillator, PLL

$$f_{LO} = f_0 + k\, f_{ch}$$ Channel selection

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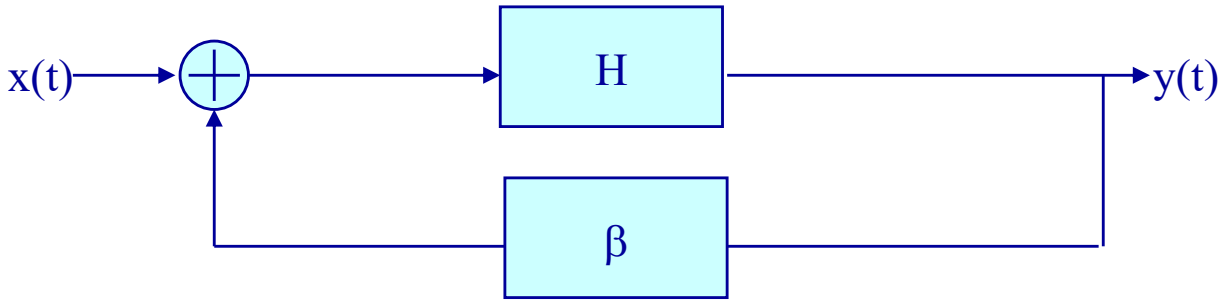
Summary

- Digital Transceiver RF Front-end
- Signal Integrity
- Frequency Synthesizers
- RF oscillators
- PLLs
- **Indirect frequency synthesis**

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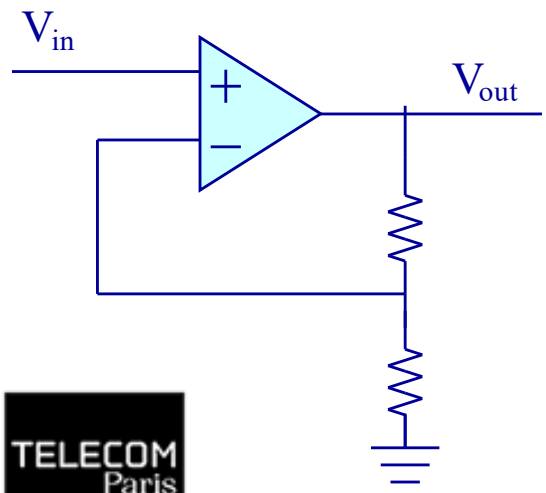
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Frequency multiplication

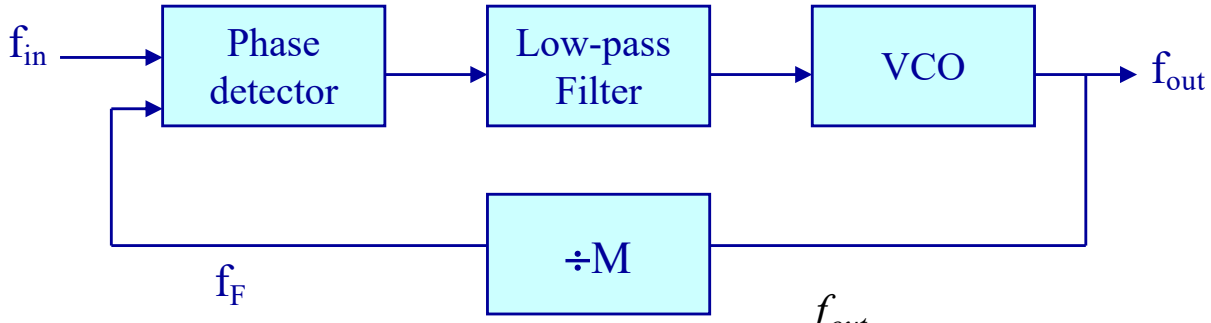


$$\frac{y}{x} = \frac{H}{1+\beta H} = \frac{1}{\beta}$$

Basic loop system



Voltage amplifier



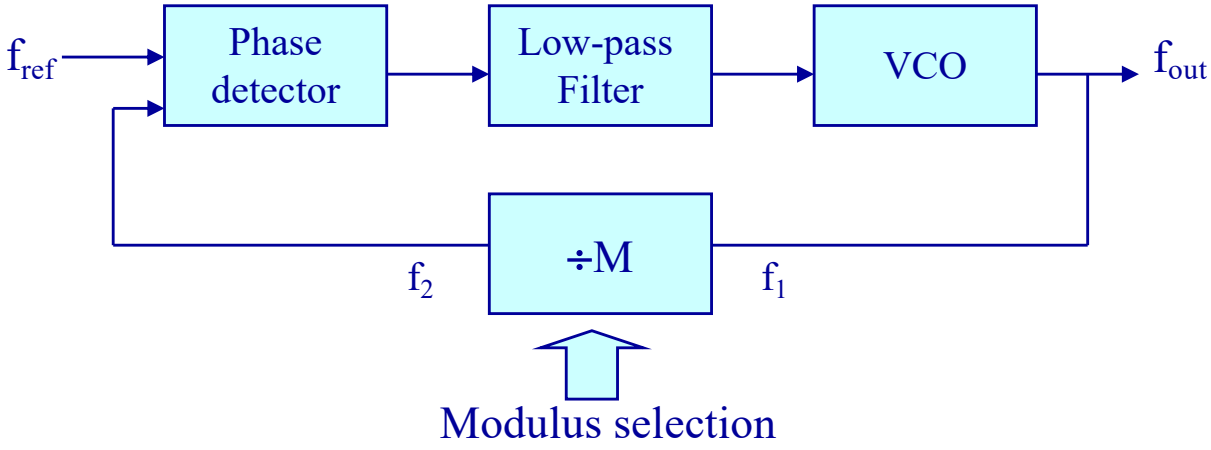
$$\frac{f_{out}}{f_{in}} = M$$

Frequency multiplier

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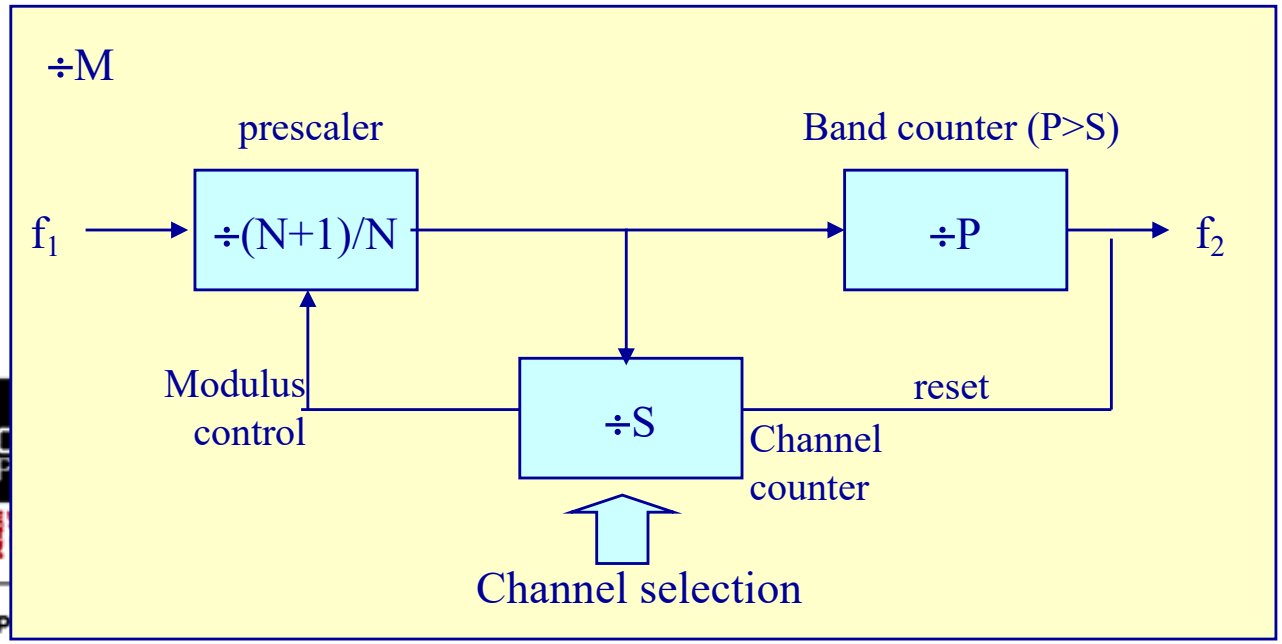
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Integer Modulus Synthesizer



$$f_{out} = Mf_{réf} = f_0 + kf_{ch}$$
$$M_L \le M \le M_H$$
$$f_0 = M_L f_{réf}$$
$$f_{ch} = f_{réf}$$

The reference input frequency must be equal to the channel spacing.

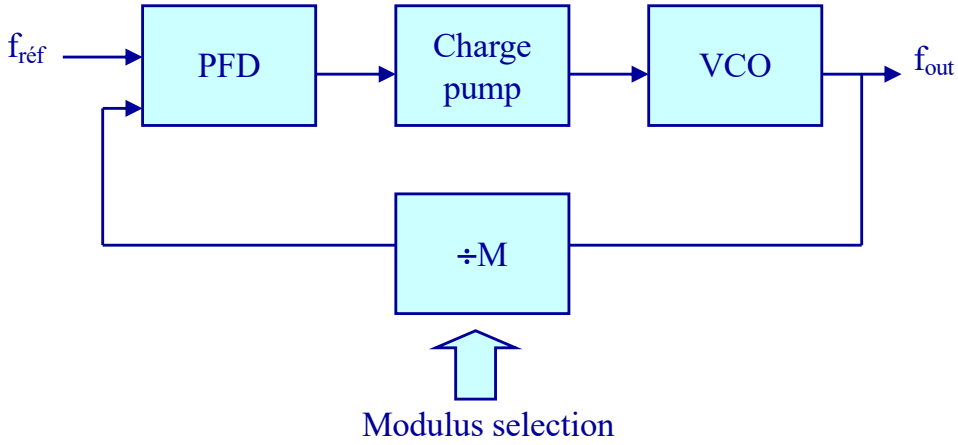


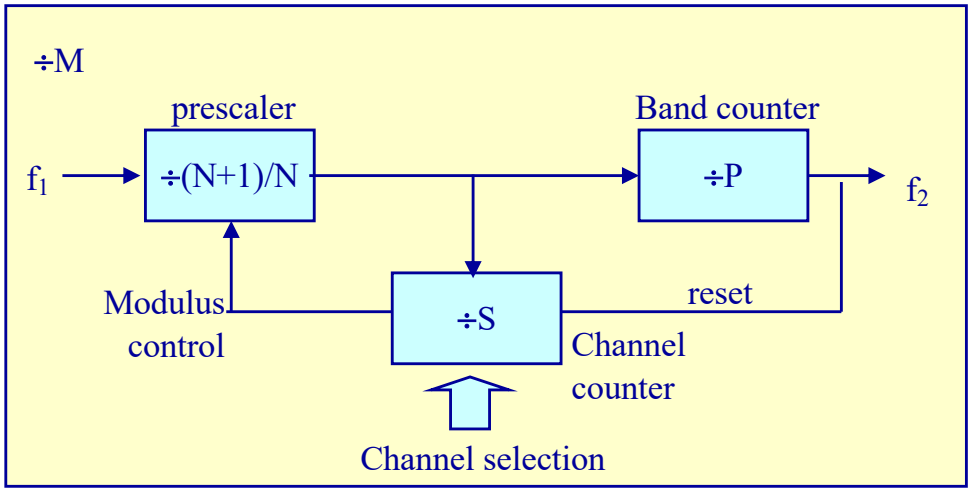
Frequency divider by pulse counting

One output cycle occurs at the end of (N + 1) * S + N * (P-S) input cycles.

$$f_2 = \frac{f_1}{NP + S}$$

Integer Modulus Synthesizer





- *Main advantage*: architecture simplicity

- *Implementation* in RF system :

Band counter, channel counter, PFD, charge pump

VCO
prescaler

} a single die in deeply submicronic CMOS technology

- *Main drawback*:

The reference frequency has a small value.
The bandwidth of PLLs is limited to 1/10 of the input frequency to ensure stability

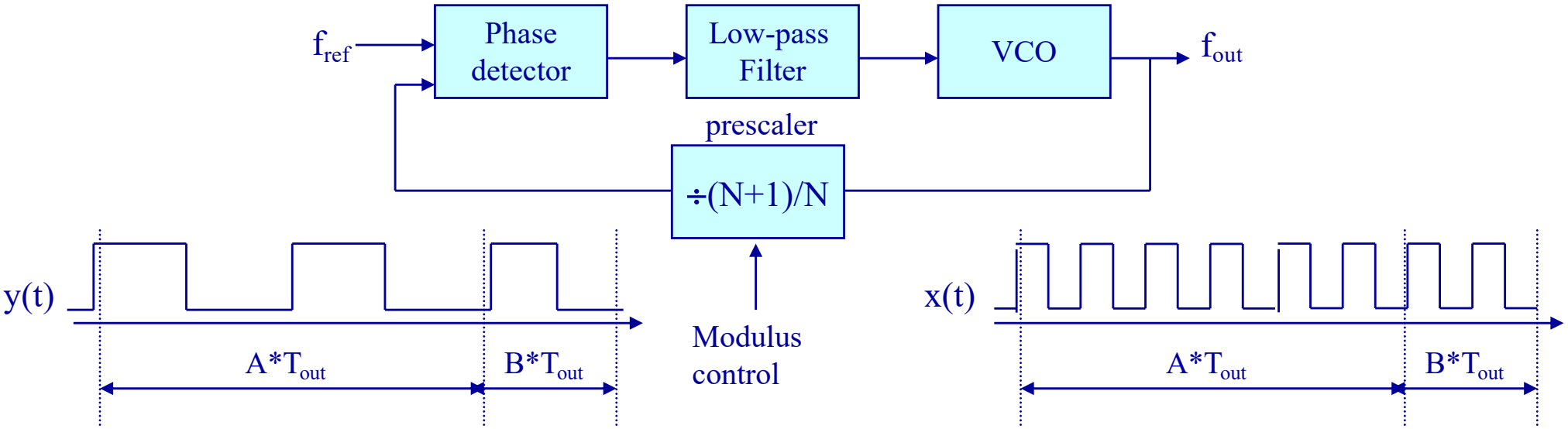
} The bandwidth of the loop is limited!

ex : GSM inter-channel spacing : 200kHz
Settling time 100 µs or more

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Fractional Modulus Synthesizer



Number of pulses during the time $(A+B)T_{out}$:

$A/(N+1) + B/N$

'Average' or equivalent frequency of y(t) :

$(A/(N+1) + B/N) \ / \ ((A+B)\ T_{out})$

$= f_{out} / M$

Locked loop :

$f_{réf} = f_{out} / M$

$f_{out} = M * f_{réf}$

$$M = \frac{A+B}{\frac{A}{N+1}+\frac{B}{N}}$$

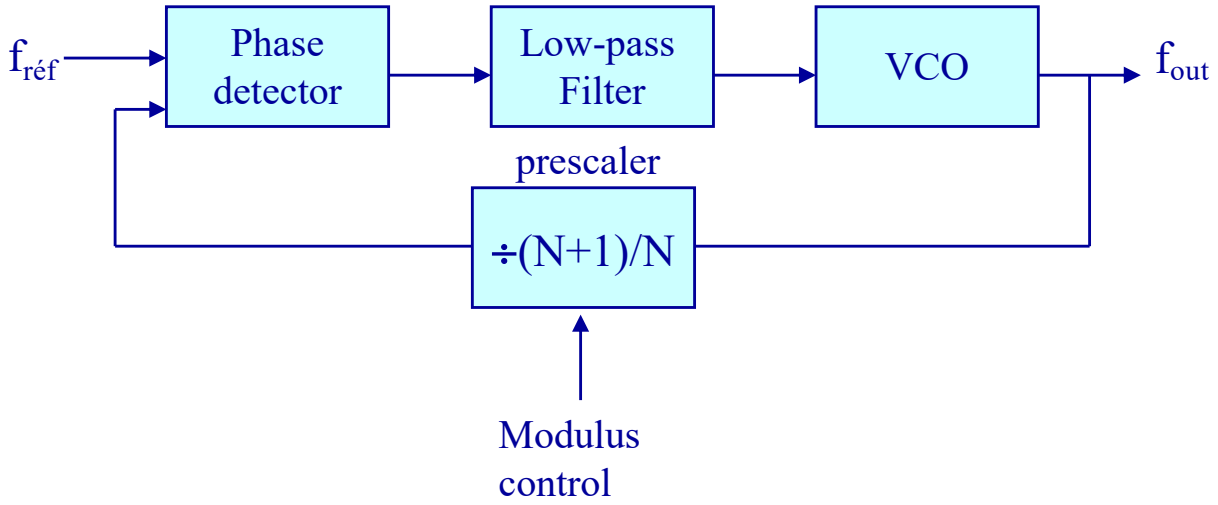
$$N < M < N+1$$

Use of a two-modulus frequency divider

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Fractional Modulus Synthesizer



EXAMPLE :
Let's Consider a synthesizer for which the reference frequency is provided by a 1MHz oscillator. The expected output frequency is:

$$f_{out} = f_0 + kf_{ch}$$

with f_0=10 MHz and f_{ch}=100kHz for k= 0, 1, 2,…9, 10.
What is the value of N?
What are the minimum possible values for A and B
to address the different channels?

?

Modulus Randomization and Noise Shaping

- Periodic switching between N and N+1 creates a cyclic phase error that generates unwanted spurious lines, known as fractional spurs.

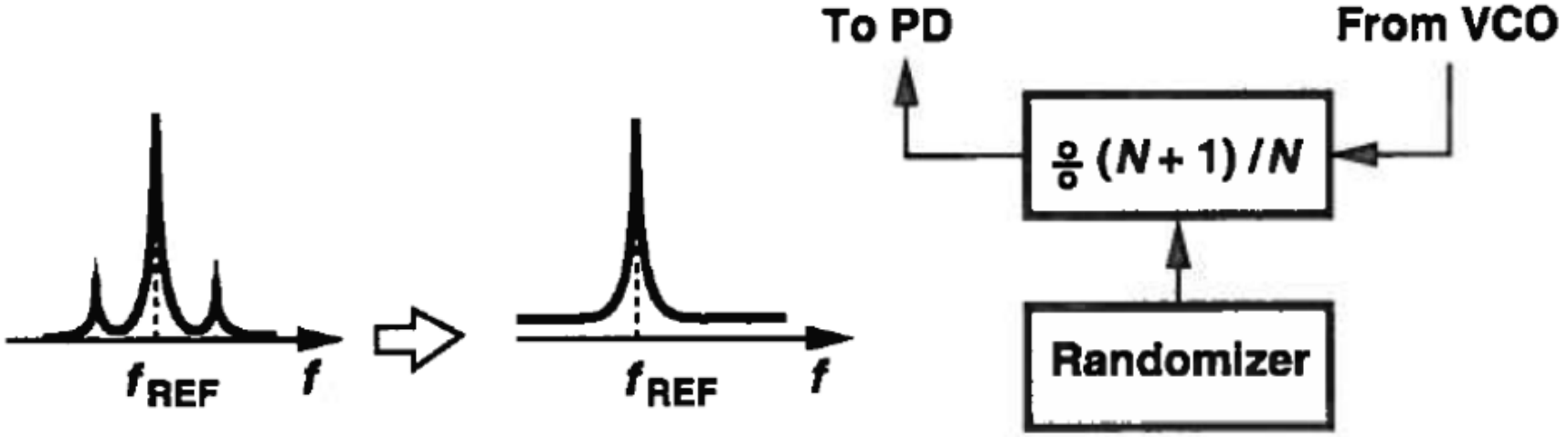
- To eliminate this problem, modern architectures incorporate a Sigma-Delta (ΣΔ) modulator (often of the MASH type).

- This modulator will desynchronize/randomize the choice of division modules to transform discrete spurious lines into continuous background noise (white noise).

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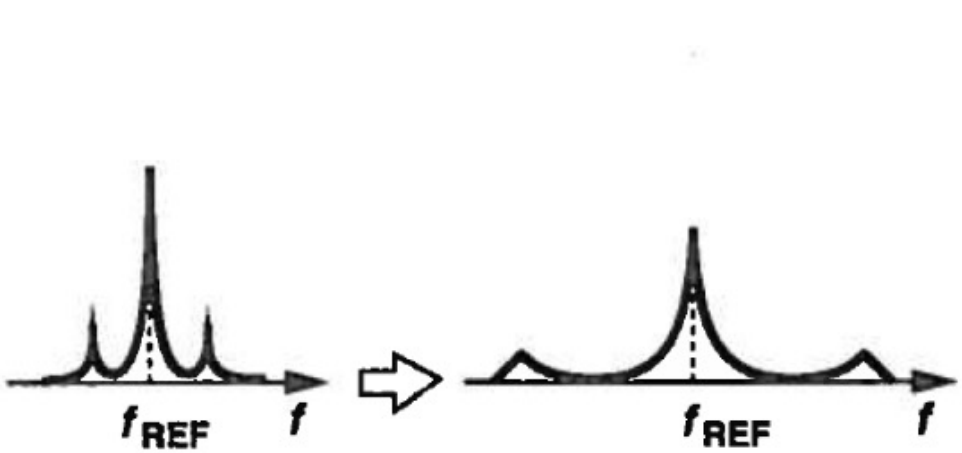
Spur Suppression with Modulus Randomization

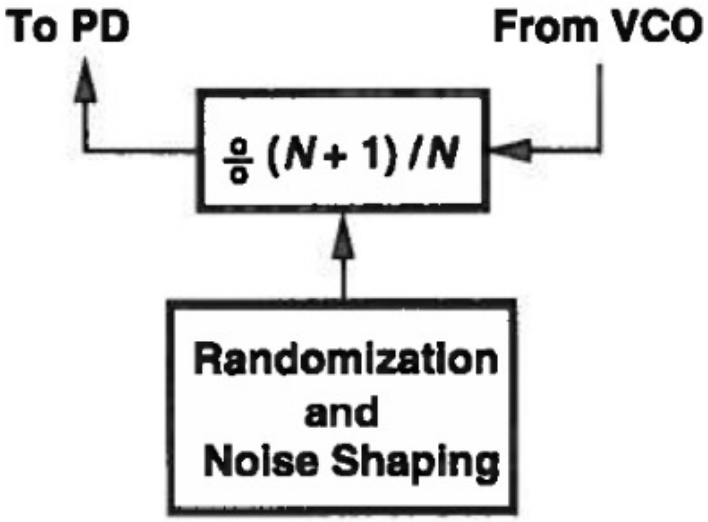


- Instead of periodically changing the divider modulus, randomly switch it such that the average division factor still yields the desired fractional value

- This converts the systematic fractional spurs into random noise

Including Noise Shaping in Modulus Control



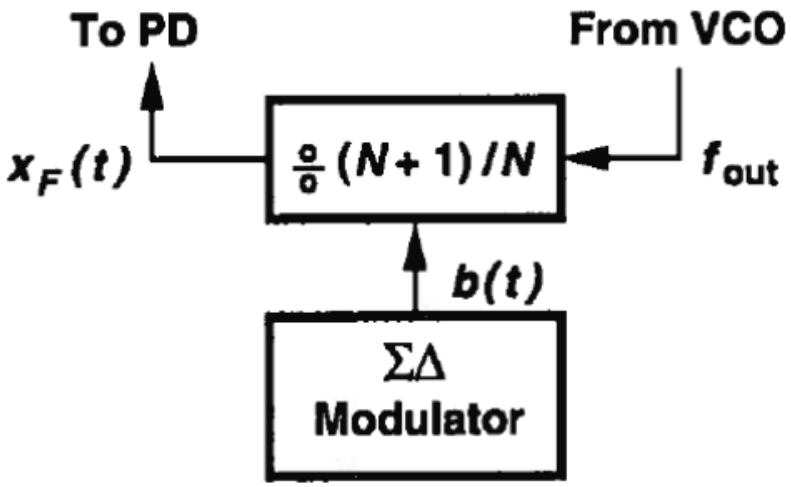


- This technique can be extended by in addition to randomization, shaping the noise in such a way that it can be filtered by the PLL

Sigma-Delta Modulation Noise Shaping

- High-pass noise shaping can be realized by using a sigma-delta modulator for modulus control

- The divider quantization noise can then be filtered by the PLL more efficiently



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Delta–Sigma Modulation in Fractional-N Frequency Synthesis

Tom A. D. Riley, *Member, IEEE*, Miles A. Copeland, *Fellow, IEEE*, and Tad A. Kwasniewski, *Member, IEEE*

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Summary of operational characteristics

characteristic	Integer Modulus Synthesizer	Fractional Modulus Synthesizer
Channel spacing	Equal to f_{ref}	Equal to f_{ref}/M (very fine)
Loop bandwidth	Narrow (stability limited to $< 0.1 f_{ref}$)	Wide (thanks to a high f_{ref})
Switching speed	Slow	Very fast
Main issue	High in-band phase noise	Fractional spurs and quantization noise

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Conclusion

- For very high frequency RF synthesizers, PLLs are preferred to DDS
  - The VCOs can deliver GHz easily

- Moreover Indirect Synthesis has excellent close-in-phase noise near the carrier frequency thanks to :
  - thanks to the spectral purity of its reference oscillator (typically a quartz crystal)
  - and the low-pass filtering action of the loop ((VCO high-pass filtering)

- Fractional Modulus Synthesizer reach the best performances in term of Channel spacing, Loop bandwidth and Switching speed at the price of increased complexity in order to reduce fractional spurs and quantization noise

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